AN AUTOMATED OIL TANK FLAW DIAGNOSIS OF IMAGES AND IMPLEMENTATION IN FPGA

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Abstract: In the every industrial diagnosis the flaw of human. But some time it is failure to diagnose the flaw. For diagnosis the flaw using the images and improvement of the VLSI technology FPGA is a hardware solution. The Proposed method flaw detected by the edges using distributed canny edge detector and to separate the flaw by applying the morphological operators. The distributed canny algorithm is like to the canny edge algorithm, but additionally introduces adaptive Thresholding to finds threshold value for block of images. In proposed edged detector reduces the latency time, and it finds the edges clearly. The output is implemented on Spartan 3E board and verifies the time for both MATLAB and XILINX.

Keywords: Flaw, Threshold, Distributed canny edge detector, Morphological operator, FPGA.

1. INTRODUCTION

The image processing is used in medical, satellite, and industrial domain. In the industrial domain, quality, and instrument faults, flaw are to diagnose by the images.so many algorithms are proposed in image processing. In oil tank industries faults may be identified by the human, it takes lot of time; sometime minor flaw detection is a failure. Existing flaw identification is explained below. Normally oil tank flaws can by identified by NDT testing, this testing needs more expansive, so proposing the image analysis pattern to diagnosis the flaw by image. Oil tank flaw identification is important one, it preventing leakages and explosion. The computer vision technology provides affordable way to detect flaws by oil tank image [1].The automated detection of flaw diagnosis establishing reliable results without human operator.

Image segmentation was used, and these methods are classified in edge, region and boundary detection of an image .The edge represents the discontinuity in the pixel, the various edge detectors are Roberts, Sobel, Prewitt, Canny [1]. The Region segmentation similarity pixels are grouped .Darwish producing the visual pattern analysis for detect the damages in the machines[2].Perener developed the inspection system for automatic defect classification system for industries [3].The developing system to identified the crack by image segmentation methods, however the improvement of the computer vision has develop system by images[4].

Developing of new technology in real world gives hardware solution for images [6], the process image on FPGA board and yields better results than MATLAB. H.Ng developing his working on defect detection by thresholding on image, but using thresholding method, higher threshold value leads the image blur, and increase latency time [7]. Ibrahim Z and Indera Putera S.H, whose develops the defect classification on PCB boards by using Morphological operators [11] .The morphological operator is only extract the image information only, noisy image is not suitable. G.M.Atiqur rahaman and M.Mobark hussain et al describe the algorithm to detect the defect in ceramic tiles. Here using the compare with original and sample image to detect the faults. It provides 93% efficient to detect the faults.

Prachip P,londe and S.A.Chavan et al describe the PCB board faults in images by using image subtraction and matching algorithm detect the faults, but some faults are not detected .An existing method of edge detectors is not suitable for Noisy input image.so it is not suitable for flaw diagnosis. The canny edge detector is suitable for noisy image, but its latency time is high, because it cannot use in real time applications [14].An affordable way to detect the flaw by image processing techniques like distributed canny edge detector and morphological operators.

2. PROPOSED METHOD

The proposed method flow chart is shown figure1. First the input image is converted into gray scale image; applying the distributed canny edge detector to find edges, and erosion and dilation morphological operator is to separate the flaw in images.

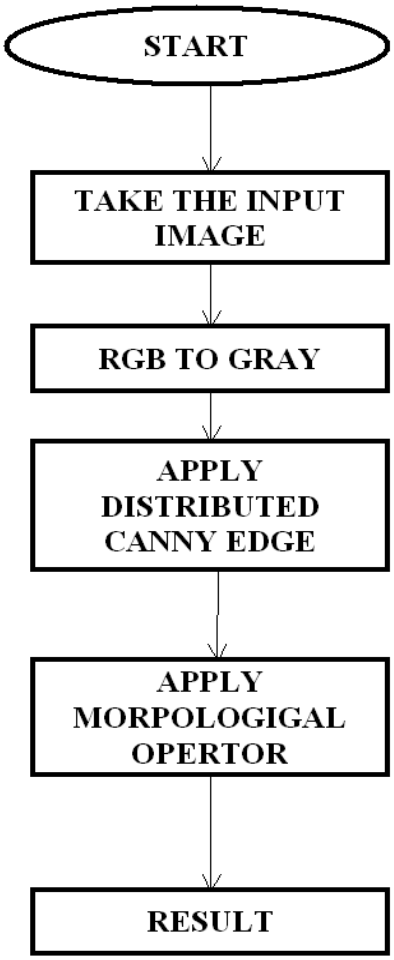

Figure 1: Flow Chart

2.1 Distributed canny edge detector

The distributed canny edge detector [14] block diagram is shown figure b. in the distributed canny edge detector the MxM image is split into NxN non-overlapping images. Each block is processed independently. The block image processing, reducing the time and increase the output efficiency, the blocks of adjacent are overlapped. In a first step to calculate the horizontal and vertical gradient from the image, and combined it. NMS–Non Maximal Suppression to thin the edge .the adaptive Thresholding to calculate the threshold value of the edge. It overcomes the manual threshold calculation.

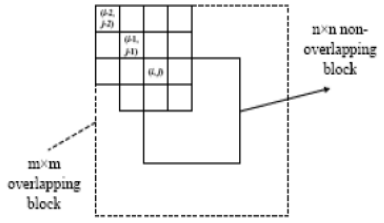

Figure 2: Image Block splitting

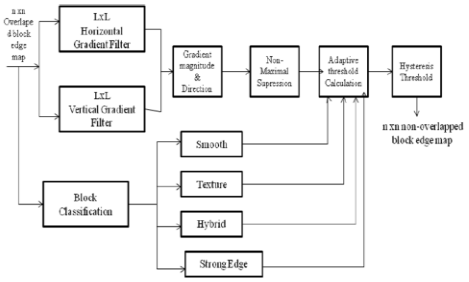

Figure 3: Block diagram of distributed canny edge detector

The block classifies the texture, strong edge, smooth, hybrid edge and adaptive Thresholding runs in continuous processing. The Block splitting diagram is shown figure2.The block diagram of the distributed canny edge detector is shown figure3.The thresholding values are calculated based on the minimum and maximum value of the image pixel. The distributed canny Detector is similar to canny edge detector, first process is applying Gaussian filter which removes the noise in the image. After that gradient values to be calculated .NMS is to thin edges and continuous execution of block classification and adaptive thresholding reduce the time, finally the hysteresis thresholding maps the edge for combining blocks.

2.2 Erosion and dilation

Erosion generally shrinking .Gray scale images, containing 0 and 1.0 represents the dark area, 1 representing a white or bright area. Each background pixel that has a neighbor in the object is relabeled as an object pixel. Making image object bigger, also called

growing. It adds pixel in the boundaries of the object. The dilation operator calculating flaw pixel to expand it, after that the closing operator filter the noise and separate the flaw.

3. RESULTS AND DISSCUSSION OF IMAGE PROCESSING

The input image and gray image are shown in figure4.The gray conversions are easy process because it contains only the zeros and ones. Second figure5, shows the distributed canny edge detector output, that is used to find the large intensity occur in the input image. In distributed canny edge detector process the image into splitting the blocks. Third step to apply the morphological dilation and closing operator to get flaw in the output image. That is shown in figure6.

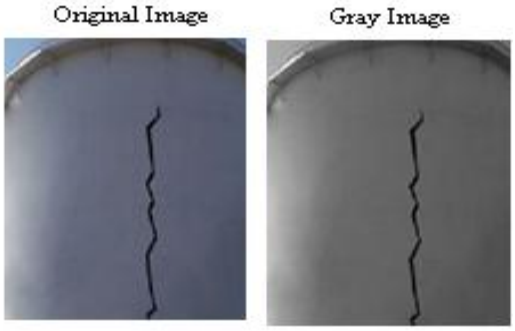

Figure 4: Input and gray image

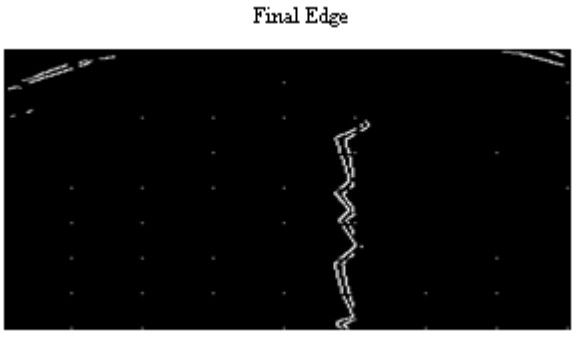

Figure 5: Distributed canny edge detector output

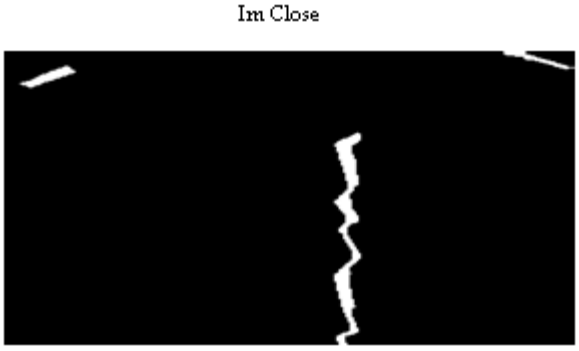

Figure 6: flaw output

4. FPGA

FPGA is Field programmable gate array can be designed for user requirements, because it is programmable. FPGA has also an excellent performance compared to other processors. It has a high computational density, high speed, low power consumption and less time to process. FPGA can be processed using the LUT (Look up Table), Multipliers, MUX, and flip-flops.FPGA is also an efficient performance than CPLD (Complex programmable logic device), PLD (Programmable logic device), and PLA (Programmable logic array).The working ability of FPGA device is high because changing the operation of the device. FPGA technology has allowed thevarious application areas to process likewise video surveillance, medical field, object identification, etc…The FPGA manufactured by several vendors that are Xilinx (Spartan3E), Altera Quartus; Virtex etc…Each FPGA structures different and processing speed also differ .In Xilinx ISE tool performing the timing analysis, RTL diagram, synthesis and finally configure the FPGA.

5. FPGA IMPLEMENTAION

Proposed of the FPGA hardware block diagram is shown in figure7.The input image should be converted into text format and then given into Xilinx. The code may be written in VHDL or Verilog. The block diagram image text and conversion is in figure8.this system consist the two sections.

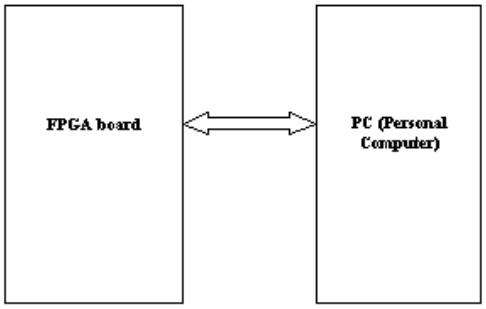

Figure 7: Block diagram of FPGA system

The first one is a PC (Personal Computer), FPGA, It needs serial and parallel cable to transfer the files image and shown the output. Dumping the VHDL code into the FPGA board before the image to text conversion is needed because FPGA accepts the digital inputs only.

Applying the algorithm to verify the flaw in the image, the distributed canny edge detector and morphological operation processed in FPGA. Thereafter the process is complete, when the MATLAB converted the text file to image format. The output result is shown in the monitor screen of computer.

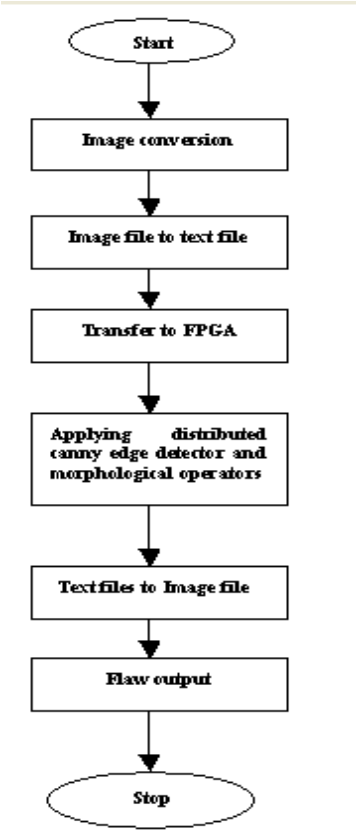

Figure 8: Flow chart for FPGA implementation

6. FPGA RESULTS

The proposed system of FPGA hardware kit is shown in the figure9.The FPGA board consisting the ROM ,RAM, flip-flops, LUTs and multiplexer. The text file conversion diagram given in figure10.the text file can be transferred by the serial cable port. In FPGA process the text files and synthesized in Xilinx ISE software. The summary of the resultant image is shown in figure11.in summary reports the debugging of the software code, if any, error in the code, it shows to correct it. Finally the summary report tells the no error, no warning to implementing the code to the FPGA. The report also creates the RTL (Register Transfer Level) schematic diagram.

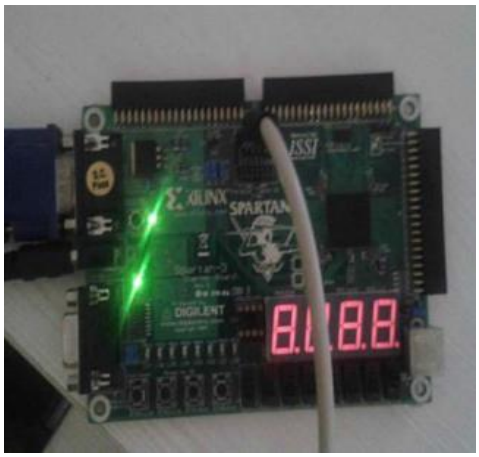

Figure9: Spartan 3E kit

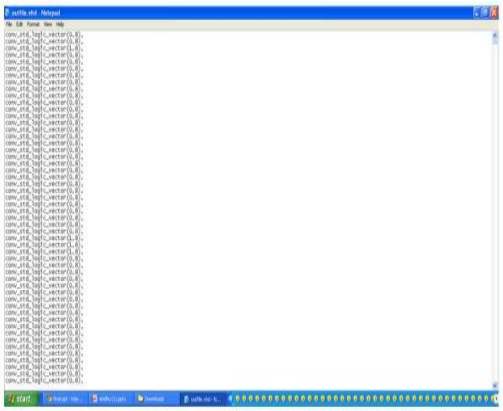

Figure 10: Text files, data for input image

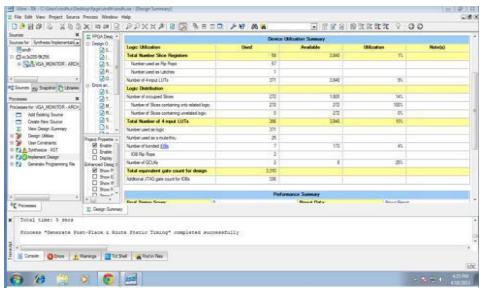

Figure 11: Summary of the input image

The flaw output occurs in the PC screen. The result of FPGA implementation is shown figure 12.After that to calculating the time for Xilinx software.to compare the result with MATLAB.

Figure 12: Output image

7. CONCLUSION

The Proposed algorithm of distributed canny and the operator reduce the latency time and improve the efficiency edge detection. This proposed algorithm is suitable for real time object identification. This algorithm is used to find the tumor in the computer tomography images The distributed canny detector improve the efficiency to detect the edges clearly, so first step of processing easily diagnosis the flaw pixel. The Morphological operator which is separates the flaws from the image. These propose system used for real time surveying, Segmentation .In future scope we using the fuzzy clustering and classifiers, instead of Spartan 3E various FPGA boards to compare the time.

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