A COMPARATIVE ANALYSIS OF HIGH SPEED DYNAMIC COMPARATOR IN 180NM AND 90NM USING H-SPICE

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Abstract: Now-a-days power generation is a big problem. To achieve the power consumption scaling is important in all circuits. Comparator is one of the components most importantly required in Analog to digital converter. In this paper, we present a comparative analysis of high speed dynamic comparator in various scaling ranges such as 180nm and 90nm. A comparison can be performed among various circuit parameters. The main parameters considered in the performance analysis are delay and power consumption. H-Spice simulation software is used for design and analysis of the dynamic comparator circuits in the above specified scaling range. Finally functionality of the proposed comparator is checking via Quatrus Kit in Verilog coding.

Keywords: Dynamic comparator, ADC, H-Spice, 90nm.

1. INTRODUCTION

Comparators have essential influence on the overall performance in high speed analog to digital convertors (ADCs). In wide-ranging a comparator is a device, which compares two currents or voltages and produces the digital output based on the comparison. Since comparators are usually not used with feedback, there is no need for compensation so neither the area reduction or speed reduction value is invited. Comparators are known as 1-bit analog to digital converter and for that reason they are mostly used in large quantity in A/D converter Dynamic comparators are widely used in the design of high speed ADCs. Due to speed, low power consumption, dynamic latched comparators are very attractive for many applications such as high-speed ADCs, memory sense amplifiers (SAs) and data receivers. High speed flash ADCs, need high speed, low power and small chip area. The designed dynamic latch comparator is required for high-speed analog-to-digital converters to get faster signal conversion and to reduce the power dissipation, which is protected to noise. However, since this comparator has two tail transistors which limit the total current flowing through the both of the outputs, it shows strong dependency of speed and offset voltage with different common-mode input voltage. To overcome this drawback, the comparator with separated input-gain stage and output-latch stage was introduced.

The structure of double-tail dynamic comparator is based on design of a separate input and latch stage. This separation enables fast operation over a wide common-mode and supply voltage range. The conventional double-tail comparator does not require high voltage or stacking of too many transistors. A conventional double-tail comparator has less stacking and then can operate at lower supply voltages compared to the conventional dynamic comparator. Basically by adding a few minimum-size transistors to the conventional double-tail dynamic comparator, latch delay time is reduced. This is also results in considerable power savings when compared to the conventional double-tail comparator. In this paper, a comprehensive analysis about the delay and power of dynamic comparators has been presented for various architectures.

The rest of this paper is organized as follows. The Section II investigates the existing dynamic comparators. Delay analysis is also presented. The proposed comparator is presented in Section III. Section IV shows Simulation results and performance chart, followed by conclusions in SectionV.

2. EXISTING COMPARATORS

Clocked regenerative comparators have found wide applications in many high-speed ADCs since they can make fast decisions due to the strong positive feedback in the regenerative latch. Single tail comparator and conventional double tail dynamic comparator are the existing comparators.

2.1 Single Tail Comparator

The Circuit diagram of the Single tail comparator is shown in Fig.1. It is mostly used in A/D converters,

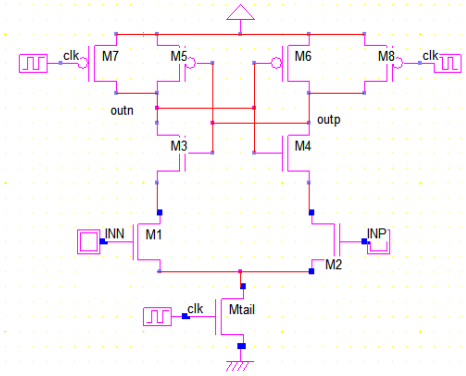

Figure 1: Single tail comparator

with high input impedance, no static power dissipation and rail-to-rail output swing. The operation of the comparator can be explained by using two Phases. When Clk=0, this circuit operates in reset phase. In this phase, Mtail transsitor get off and reset transistors (M7 and M8) pull both output nodes Outn and Outp to VDD to indicate a start condition and to have a valid logical level during this phase. when CLK = VDD, this circuit operates in comparison phase, transistors M7 and M8 are off, and Mtail is on. Outp, Outn which had been pre-charged to VDD and start to discharge with different discharging rates depending on the corresponding input voltage (INN/INP). Let us consider the case where VINP > VINN, Outp discharges faster than Outn, when Outp falls down to VDD–|thresholdvoltage pmos| well before Outn, the corresponding pMOS transistor (M5) will turn on initiating the latch regeneration caused by inverters in back-to-back connections (M3, M5 and M4, M6). Thus, Outn pulls to VDD and Outp discharges to ground. If VINP < VINN, the circuits works vice versa. The total delay of single tail comparator is as follows
tdelay = t0 + tlatch t0 represents the discharging delay
tlatch represents the latching delay.

This structure has the following advantages such as higher input impedance, no static power consumption and rail-to-rail output swing. There are two drawbacks are presenting in this circuits such as several stacking, due to the several stacking high supply voltage is needed for its operation. Another drawback of this circuit is there is only one current path.

2.2 Conventional Dynamic Double Tail Comparator

A conventional double-tail comparator is shown in Fig.2.This topology has less stacking and so it can operate at lower supply voltages compared to the single tail comparator. The double tail enables both a large current and smaller current in the latching stage for fast operation and input stage for lower offset respectively.

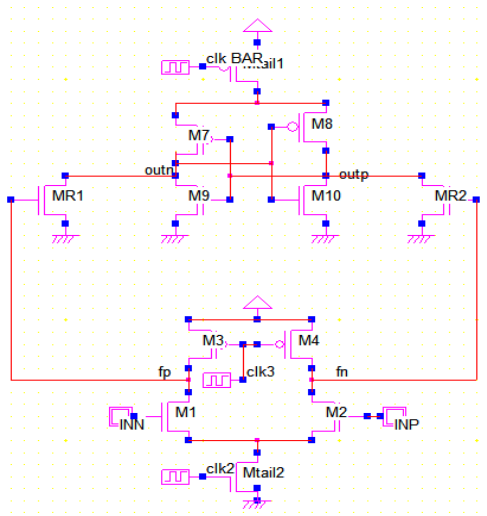

Figure 2: Conventional dynamic double tail comparator

The operation of this comparator is as follows, when CLK = 0, this circuit operates in reset phase. In this phase, Mtail1 and Mtail2 are off, transistors M3 and M4 precharge fn and fp nodes to VDD, which causes transistors MR1 and MR2 to discharge the output nodes to ground. In decision-making phase or comparison phase, CLK =VDD, Mtail1 and Mtail2 gets on, M3 and M4 turn off and voltages at nodes fn and fp start to drop with the rate defined by Mtail1 current/Cfn(p) and on top of this, a ΔVfn(p) will build up. The intermediate stage formed by MR1 and MR2 passes ΔVfn(p) to the cross coupled inverters and also provides a good shielding between input and output, resulting in reduction of kickback noise. Similar to the single tail comparator, the delay of this comparator consists of two parts can be explained in below such that The delay t0 represents the capacitive charging of the load capacitance at the latch stage output nodes such as Outn and Outp until the first n-channel transistor (M9 or M10) gets on, after which the latch regeneration starts; thus t0 is obtained. After the first n-channel transistor of the latch turns on, the corresponding output will be discharged to the ground, leading front p-channel transistor (M8) to turn on, charging another output (Outp) to the VDD. The regeneration time (tlatch) is achieved.

The initial voltage difference is

$$\Delta V_0 = V_{\mathrm{Thn}} \frac{\Delta I_{\mathrm{latch}}}{I_{\mathrm{B1}}} \approx 2V_{\mathrm{Thn}} \frac{\Delta I_{\mathrm{latch}}}{I_{\mathrm{tail2}}} = 2V_{\mathrm{Thn}} \frac{g_{\mathrm{mR1,2}}}{I_{\mathrm{tail2}}} \Delta V_{\mathrm{fn/fp}}$$

Thus, we will be concluded that two important parameters which influence the initial output differential voltage (ΔV0) are the trans conductance of the intermediate stage transistors and the voltage difference at the first stage outputs like fn and fp at time t0.

3. PROPOSED DYNAMIC DOUBLE TAIL HIGH SPEED COMPARATOR

Fig.3. describes the schematic diagram of the proposed dynamic double-tail high speed comparator. Due to the better performance of double-tail architecture in low-voltage purposes, the proposed comparator is designed based on the double-tail structure. The main idea of the proposed high speed comparator is to increase ΔVfn/fp to increase the latch regeneration speed. For this reason, two control transistors (Mc1 and Mc2) have been added to the first stage in parallel to M3 or M4 transistors.

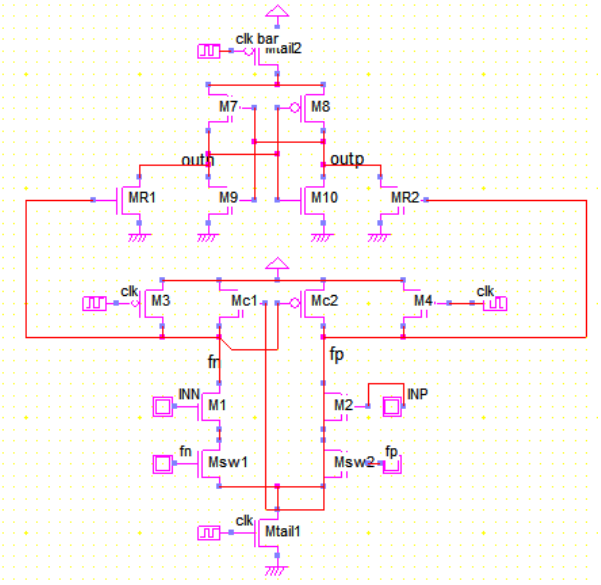

Figure 3: Proposed dynamic double tail high speed comparator

The operation of the proposed comparator is as follows, when CLK = 0, this circuit operates in reset phase. In this phase, Mtail1 and Mtail2 are off. It will be avoiding static power consumption. M3 and M4 pulls both fn and fp nodes to VDD, hence transistor Mc1 and Mc2 are gets off. Intermediate stage transistors (MR1 and MR2) reset both latch outputs to ground. In decision-making phase, CLK = VDD, Mtail and Mtail2 are gets on, transistors M3 and M4 turn off. Further at the beginning of this phase, the control transistors are still in off state.

Thus, fn and fp start to decrease with different rates according to the input voltages. Suppose VINP is greater than VINN, fn decrease faster than fp. As long as fn continues decreasing, the corresponding pMOS control transistor (Mc1) starts to turn on, pulling fp node again back to the VDD; so another control transistor (Mc2) is remains in off condition, allow fn to be discharged fully. In another words, unlike conventional double-tail dynamic comparator in proposed high speed comparator, ΔVfn/fp is just a function of input transistor trans conductance and input voltage difference. The proposed structure as soon as detects that for instance node fn discharges faster, a pMOS transistor (Mc1) turns on, pulling the other node fp again back to the VDD. Therefore, the voltage difference between fn and fp (Vfn/fp) will raises in an exponential manner, leads to the reduction of latch regeneration time. Despite of this advantages in the proposed idea, there is a drawback will be in this structure, when one of the control transistors (e.g., Mc2) turns on, a current from VDD is drawn to the ground via input and tail transistor (e.g., Mc2, M2, and Mtail1), resulting in static power consumption. To overcome this drawback, two nMOS switches [Msw1 and Msw2] are used below the input transistors as shown in Fig. 3. At the starting of the comparison phase or decision making phase, due to the both fn and fp nodes have been pre-charged to VDD. Both switches are in closed position and fn and fp start to drop with different discharging rates. As early as the comparator detects that one of the fn or fp nodes is discharging faster, control transistors will used here to increase their voltage difference. Suppose that fn is increasing up to the VDD and fp should be discharged fully, hence the switch in the charging path of fn will be opened to prevent any current drawn from VDD. but the other switch connected to fp will be closed to allow the complete discharge of fn node. In another words, the operation of the control transistors with the switches compete with successfully the operation of the latch.

The analysis of proposed high speed comparator is similar to the conventional double-tail dynamic comparator, however; the proposed dynamic comparator enhances the speed of the double-tail

comparator by affecting two important factors: first, it increases the initial output voltage difference at the beginning of the regeneration and second, it enhances the effective transconductace of the latch.

4. RESULTS AND SIMULATIONS

The high speed comparator in 180nm and 90nm can be designed in H-spice software. By using this software various parameters can be analyzed. The transient analysis of 90nm and 180nm outputs are shown in Fig. 4 and Fig.5. The transient analysis explain the operational concepts. when clk =0 and INN> INP, the outn will be high and output wil be low.

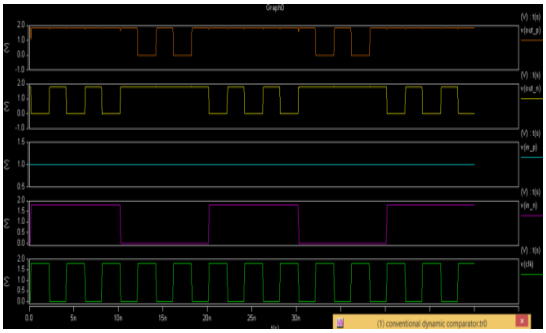

Figure 4: A Single tail comparator in 90nm

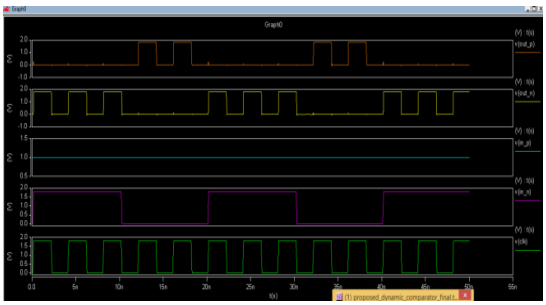

Figure 5: Conventional dynamic double tail comparator in 90nm

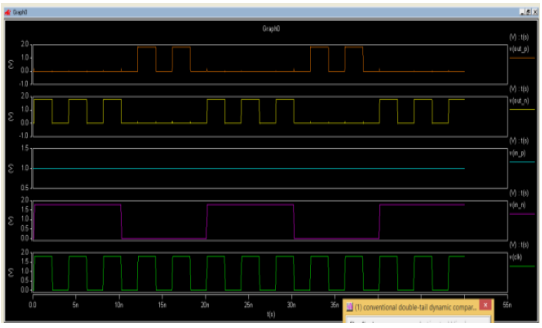

Figure 6: Proposed dynamic double tail high speed comparator in 90nm

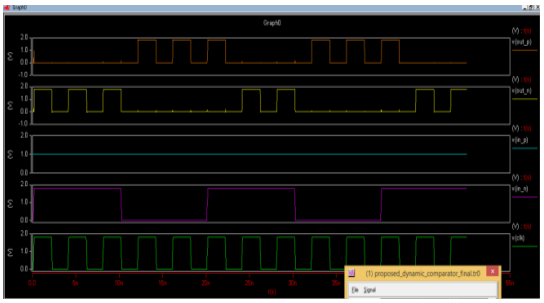

Figure 5: A Single tail comparator in 180nm

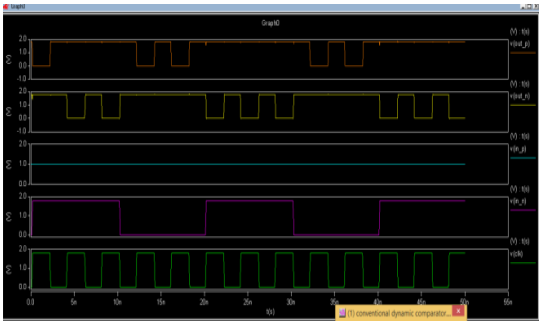

Figure 6: Conventional dynamic double tail comparator in 180nm

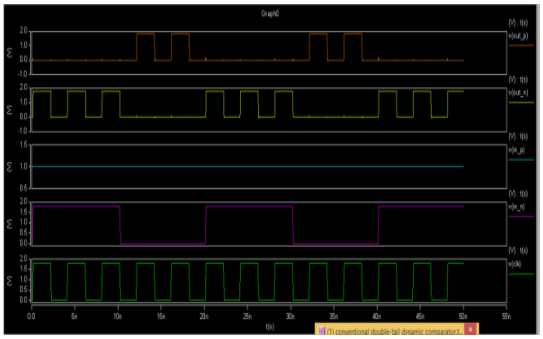

Figure 7: Proposed dynamic double tail high speed comparator in 180nm

From the performance analysis we understood that the 90nm structure has the lesser delay and the power consumption than the 180nm structure. In addition to that it can operate at lower supply voltage than the 180nm devices.

Table 1: Describes The Parameter Analysis Of 180nm Structure:

parameter	Single tail comparator	conventional double-tail dynamic comparator	Proposed double tail high speed comparator
Ivdd(Amps)	1.3860u	3.6564u	33.1045u
Tplh(sec)	6.0442n	10.1748n	10.1686n
Tphl(sec)	4.1251n	16.2098p	14.3336p
Peakpwr(watt)	160.8257u	638.3199u	564.454u
inputpp_in_n(volt)	1.8000	1.8000	1.8000
outputpp_out_n(volt)	1.8555	1.8877	1.8684
Iddrms(Amps)	9.2532u	25.8944u	56.0154u
Power(watt)	2.4024u	6.1401u	57.6570u
avg_power(watt)	2.4422u	6.4466u	5.79821u
average_delay(sec)	959.5520p	5.0793n	5.0771n
power_delay_product (j)	2.3435f	32.7444f	294.381f

Table 1 performance chart for 180nm

Table 2 describes the parameter analysis 90nm devices. From the table we could understand the delay will be reduced in 90nm than the 180nm devices:

Parameter	conventional dynamic comparator	conventional double-tail dynamic comparator	proposed dynamic comparator final
Ivdd	812.8833n	519.5155n	4.0710u
Tplh	10.0745n	10.1763n	10.1524n
Tphl	112.4145p	16.0634p	14.8008p
peakpwr	15.1807u	61.6943u	52.9807u
inputpp_in_n	1.0000	1.0000	1.0000
outputpp_out_n	1.0333	1.0458	1.0358
Iddrms	3.3292u	4.0491u	8.1575u
power	820.5723n	500.2597n	4.1266u
avg_power	823.3748n	509.0397n	4.1352n
average_delay	4.9811n	6.0801n	5.0688n
power_delay_product	4.1013f	2.5860f	2.09607f

Table 2: performance chart for 90nm

5. CONCLUSION

The High speed comparator in 90nm and 180nm has been designed using simulation software. High speed can achieve here by the way of minimizing the delay. This work presents the delay analysis for clocked dynamic comparators. Two structures of Single tail comparator and conventional double- tail dynamic comparators have been analyzed. A new high speed comparator with low-power capability has been achieved in order to improve the performance of the comparator and also reduces the delay. Finally the functionality of the high speed comparator can checked through the quatrus kit by blinking LEDS.

6. FUTURE WORK

The same structures can be implemented by using FINFET to further improve the functionality of the circuit.

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