DESIGN AND COMPARITIVE ANALYSIS OF SRAM CELLS STABILITY USING 45NM

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Abstract: Power consumption has become a critical design concern for many VLSI systems. In this paper propose a power gating technique to reduce the power and increase the stability of the cell. To increase the memory density, bit cells used reduce the area. Power consumption and speed is the important issue to minimize the power value by using cell read and stability value. This paper is also investigating the read static noise margin, write noise margin and read retention voltage. Tanner EDA tool is also used to observe the schematic solution. This method will decrease the power consumption and increase the stability of the SRAM cell.

Index Terms: SRAM, Power gating, Read retention Voltage, Dynamic Stability.

1. INTRODUCTION

In this paper we introduce some design techniques to reduce the power consumption and increase the stability f the cell. Each cell contains some transistors. Existing method we use 6T SRAM cell. Stability of the 6T SRAM cell is poor. Measuring the cell current by change cell structure. It will damage the circuit and reduce the stability and increase the losses. But in this method we accurately estimate the cell stability of the SRAM cell without modifying the cell structure. Technology scaling is used to increase the complexity of the cell design. MCML (Mos Current Mode Logic) is one of the logic design widely used for high speed circuits. In this method we use power gating and clock gating techniques.

In the existing system 32nm devices are used. The estimation results focused on the random manner. It will not display the final result. Random mismatches are occurs in the wafer. As the temperature is increases stability of the read mode and sleep mode deceases.

In the proposed method we use the Power gating to reduce the power dissipation and reduce the noise margin level. No of papers are published for estimating the noise margin. But most of the techniques are not directly applied to the SRAM cell. But this paper estimates the read and writes stability.

2. BACKGROUND

2.1 Static Noise Margin

Read static and write noise margin are the extended definitions of the SNM. These two terms are defined as the, maximum tolerable noise injected onto the cell.

2.2 Read Retention Voltage

Supply read retention voltage is highly correlated. This technique can be used to extracts the cell read stability without changing the cell structure.6T SRAM cell read stability requires to sweeping the internal nodes in order to obtain the voltage transfer curvatures. Large are used to choose the Supply Read Retention Voltage. 6T SRAM cell structure we use two CMOS inverter. Word line used to control the circuit. 6T circuit are contains Pull up and Pull Down transistors. Other two transistors are called as the access transistors.

Voltage division between the access transistor and driver transistor read stability to be low during the read operation. Leakage current is flows through the NMOS transistor. It will increase the source to supply voltage. More than one transistor is off means the path between the supply voltage to ground is equal.

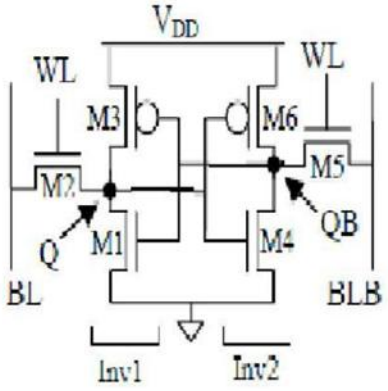

Figure 1: SRAM cell Write Stability

Random telegraph noise is occurs in 6T SRAM cell. The noise caused by the charge trapping or re trapping. SRAM transistor area will increases in the trapping method. Cell current is measured in two ways. Pull of NMOS devices and Pull down of NMOS devices additionally we used as the access transistor.

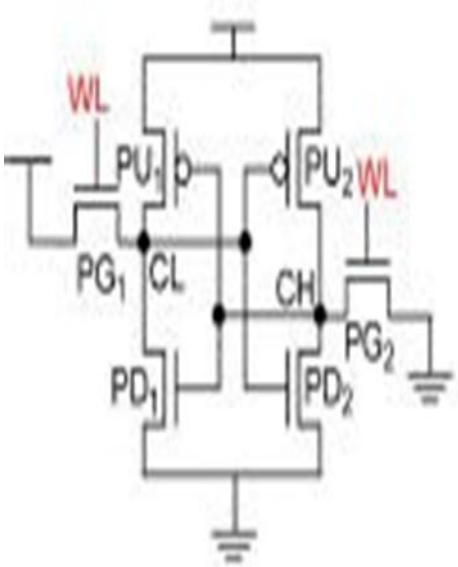

Figure 2: SRAM cell Read Stability

Most of the stable cells are measuring the pull down current. Implementing this technique in a COM SRAM chip extra cost for the area measurement without changing the cell structure. It is the biggest disadvantage 6T SRAM cell. Reduce the cost and Power dissipation and power gating Techniques.

3. MCML

Reduce the static power we use different power gating techniques source. Proposed method we use sleep transistor. Sleep transistor is inserted in series with the supply voltage or the current

Insert the sleep transistor will affect the operation voltage of the MCMLcircuits.8T SRAM structure contains 8 transistors in the single cell. N3 and N4 will denoted as the access transistors. In these transistors contains the input to the bit line. N3 performs the read operation and N4 performs the write operation.

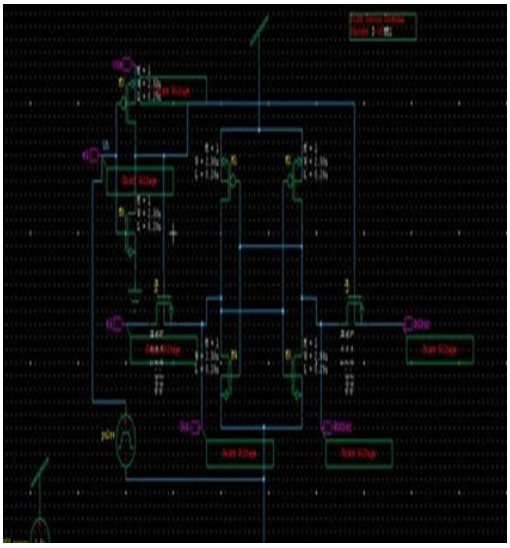

Figure3: 8T SRAM Structure

Power gating is the circuit design techniques which reduce the static power. Inserting the power switches in the supply path and it widely used in the industrial side. There are the two implemented design schemes of power gating techniques. Coarse grain power gating in which the blocks are disconnected. The sleep transistor connected internally in the standard cell. With Sleep transistor inserted in series with the supply voltage or current source to reduce by power. Power consuption of the MCML gte is independent of switching frequency, and it is given by

P=VDD*Iv.

Reducing the supply voltage is an effective method to lower the power consumption of MCML circuits. The operation of the MCML is based on the redicrecting or switching.

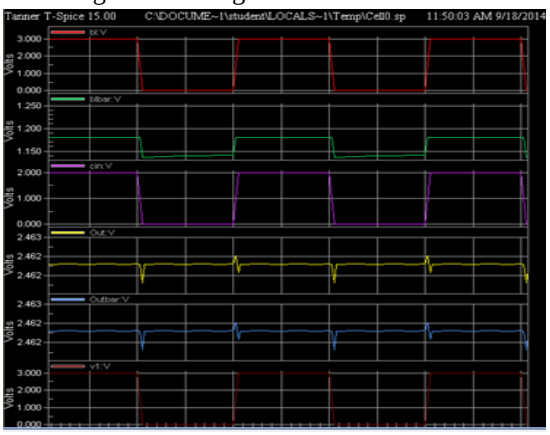

Figure4: Output Waveform of 8T SRAM cell

When applying the ON signal to the gate current source that will connects the bulk voltage to the bias voltage.

4. CONCLUSION

Standby power is the biggest drawback of the MCML circuits. The active power consumption of the MCML circuits can reduce the near threshold value. While the standby power is large. We use the power gating techniques to reduce the standby power of the circuit. Proposed method using the sleep transistor control the gate bias voltage of the current source implementation

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