# DESIGN AND IMPLEMENTATION OF MULTIPLEXER USING POSITIV FEEDBACK ADIABATIC LOGIC

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**Abstract:** Adiabatic logic is an implementation of reversible logic in CMOS where the current flow through the circuit is controlled such that the energy dissipation due to switching and capacitor dissipation is minimized. Dual-rail adiabatic logic implemented with reversible principles has also been demonstrated to significantly reduce differential power consumption. The dual-rail adiabatic logic show reduction in average and differential power, making this design methodology advantageous in applications where security is the primary design metric and operating frequency is slower, such as Smart Cards. The horizontal offsets in the permutation matrix with the necessary switches required for synthesis instead of using a library of equivalent functions. Adiabatic logic operates on switching concept. Therefore switches operate ON and OFF mode. The toffoli gate is one of the reversible gate. The dual rail toffoli gate is designed using transmission gate. The adiabatic logic is classified into two types. They are Positive Feedback Adiabatic Logic (PFAL) and Efficient Charge Recovery Logic(ECRL). In my proposed system PFAL circuit is designed and compared to the existing circuit. The design is capable of forward encryption and reverse decryption with minimal overhead, allowing for efficient hardware reuse.

**Key words:** Adiabatic logic, toffoli gate, ECRL, PFAL.

## 1. INTRODUCTION

Adiabatic logic is a design methodology for reversible logic in CMOS where the current flow through the circuit is controlled such that the energy dissipation due to switching and capacitor dissipation is minimized. Recent advances in reversible logic using and quantum computer algorithms allow for improved computer architectures. We propose the use of body biasing in CMOS adiabatic systems as a design methodology for reducing the need for gradually changing the energy barriers. Simulation results in HSPICE at 22nm are presented which shown behavior of a source-memory device operating at sub operation. Second, we address whether reversible logic can be used to design sequential computing structures, such as memory devices. We present an analysis of quantum Turing machines with sequential reversible logic structures.

A mathematical proof is presented showing bit erasure does not occur in sequential reversible logic structures, and that these devices are physically reversible as long as appropriate delay elements are inserted in the feedback paths to prevent race conditions. This proof validates implementation of sequential reversible logic towards ultra-low power computing. Next a novel algorithm for synthesis of adiabatic circuits in CMOS is proposed. This approach is unique because it correlates the offsets in the permutation matrix to the transistors required for synthesis, instead of determining an equivalent circuit and substituting a previously synthesized circuit from a library.

## 2. ADIABATIC LOGIC:

Adiabatic circuits are low power circuits which use reversible logic to conserve energy. Unlike traditional CMOS circuits, which dissipate energy during switching, adiabatic circuits reduce dissipation by following two key rules:

- Never turn on a transistor when there is a voltage potential between the source and drain.
- Never turn off a transistor when current is flowing through it.

While this is an area of active research, current techniques rely heavily on transmission gates and trapezoidal clocks to achieve these goals. There are some classical approaches to reduce the dynamic power such as reducing supply voltage, decreasing physical capacitance and reducing switching activity. These techniques are not fit enough to meet today power requirement. However, most research has focused on building adiabatic logic, which is a promising design for low power applications.

Adiabatic logic works with the concept of switching activities which reduces the power by giving stored energy back to the supply. Thus, the term adiabatic logic is used in low-power VLSI circuits which implements reversible logic. In this, the main design changes are focused in power clock which plays the vital role in the principle of operation. Each phase of the power clock gives user to achieve the two major design rules for the adiabatic circuit design.

- Never turn on a transistor if there is a voltage across it ($V_{ds} > 0$)
- Never turn off a transistor if there is a current through it ($I_{ds} \neq 0$)
- Never pass current through a diode.

Adiabatic logic is a design methodology for reversible logic in CMOS where the current flow through the circuit is controlled such that the energy dissipation due to switching and capacitor dissipation is minimized. In adiabatic circuits were shown to produce a reduction in energy dissipation of 60% at 20 MHz and 35% less energy at 100 MHz, and reversible dual-rail CMOS pass transistors.

**Types of Adiabatic Logic,**

- Fully adiabatic families
- Quasi adiabatic families

## 3. FULLY ADIABATIC FAMILIES

It should be noted that the fully adiabatic operation of the circuit is an ideal condition which may be approached asymptotically as the switching process is slowed down. In most practical cases, the energy dissipation associated with a charge transfer event is usually composed of an adiabatic component and a non-adiabatic component. Therefore, reducing all the energy loss to zero may not possible, regardless of the switching speed.

- Efficient charge recovery logic (ECRL)
- Improved efficient charge recovery logic (IECRL)
- Positive feedback adiabatic logic (PFAL)

### 3.1 ECRL

ECRL (also known as 2N-2P is based around a pair of cross coupled PMOS transistors. Their source terminals are connected to the power- clock, and the gate of each one is connected to the drain of the other. These nodes form the complementary output signals. The function is evaluated by a series of pull-down NMOS devices. In the original description, the connectivity of the PMOS transistors bulk terminals was not specified. However, experimentation has shown that better power performance can be obtained by connecting the bulk to the power-clock, as the power-clock can be recovered to a lower voltage. This improvement is not without cost, as it introduces layout constraints that require the hot n-wells of each asynchrobatic stage to be kept separated. One disadvantage of ECRL is that once the charge from the previous stage has been recovered from the gate of the NMOS devices, there is no pull-down path to ground.

### 3.2 IECRL

IECRL first described by improves ECRL with the addition of a pair of cross-coupled NMOS devices. This produces a logic family that is based around a pair of cross-coupled inverters, a structure that is identical to the storage elements in a Static RAM (SRAM). The cross-coupled NMOS devices are an improvement over ECRL because they provide a pull down path to ground that remains even after the charge is recovered from the gates of the evaluation FETs.

### 3.3 PFAL

It is also based around a pair of cross coupled inverters. However, whilst in IECRL the NMOS devices used to evaluate the function are connected between the outputs and ground, in PFAL, these evaluation NMOS devices are connected between the outputs and the power-clock. The similarities between PFAL and IECRL gates are such that IECRL gates can be easily converted into PFAL gates. This is done by re-labelling the outputs so that their assertion levels are swapped, and connecting the NMOS evaluation devices between the power-clock and the outputs rather than between ground and the outputs

## 4. QUASI ADIABATIC FAMILIES

A quasi adiabatic process is a thermodynamic process that happens infinitely slowly. No real process is

adiabatic, but such processes can be approximated by performing them very slowly. Any reversible process is necessarily a quasi-adiabatic one. However, some quasi adiabatic processes are irreversible, if there is heat flowing (in to or out of the system) or if entropy is being created in some other way. An example of a quasi-adiabatic process that is not reversible is a compression against a system with a piston subject to friction although the system is always in thermal equilibrium, the friction ensures the generation of dissipative entropy, which directly goes against the definition of reversible. A notable example of a process that is not even quasi adiabatic is the slow heat exchange between two bodies at two finitely different temperatures, where the heat exchange rate is controlled by an approximately adiabatic partition between the two bodies in this case

## 5. BASICS OF DUAL-RAIL ADIABATIC DESIGN

Two rules must be followed in order to implement adiabatic logic in CMOS. First, a transistor must never be turned on when there is a voltage across it. This means that, if the voltage desired at the drain and source are different, then the transistor must be turned off. If this rule is violated, then energy is dissipated and information is lost. The second rule is that a nonzero voltage must never be applied across a transistor during any transition. If this occurs, then the internal resistance of the transistor is relatively small, resulting in a very high power spike and consequential energy dissipation. There are some classical approaches to reduce the dynamic power such as reducing supply voltage, decreasing physical capacitance and reducing switching activity. These techniques are not fit enough to meet today‟s power requirement. However, most research has focused on building adiabatic logic, which is a promising design for low power applications.

Dual-rail logic was implemented as a design methodology for mitigation of differential power analysis (DPA) attacks. By using dual-rail logic, special instructions may be coded in order to provide data independence from the switching activity of the circuit. Energy balancing is address in dual-rail logic by incorporating spaced between adjacent clock cycles, which guarantees all gates switch in every clock cycle. The main drawback to the dual rail approach is that there is more logic, which requires a greater number of gates, which increases both area and power consumption. Additionally, spacers and negative gate optimization is required to implement a dual-rail circuit that successfully masks power signals. Pass transistor and adiabatic logic schemes have been used to mitigate DPA attacks, but never concurrently. In multiple adiabatic implementation methodologies such as CSSAL, SYAL, 2n2p, and ECRL to design low power s-boxes.

The CSSAL showed significant improvement over the other methods at 0.18 μm. And in a charge-sharing symmetric adiabatic logic (CSSAL) was used to improve upon the energy imbalance of the s-box. Dual-rail asynchronous circuit just uses a completion detector as handshake control circuit at each stage, and the overhead of explicit storage elements are all removed. The problem is that, such efficient design is realized at the expense of dual-rail overhead and the overhead of the completion detector is quite large, which cause it Inapplicable at large function block design. This paper proposes a new asynchronous circuit design Method that uses a mixture of dual-rail and single-rail logic. The data detectability of dual-rail logic is used to realize the efficient pipeline architecture same as the dual-rail asynchronous Circuit, and single-rail logic is applied to achieve Small overhead in logic block. In the conventional dual rail

Asynchronous circuit, the completion detector needs to generate a total done signal by detecting the entire data paths of a function block. Single-rail logic in our design represents single-rail dynamic logic which is necessary to realize the efficient latch-free architecture. Compared to dual-rail logic, single-rail logic has smaller logic overhead. The truth part of dual-rail logic can be used as single-rail logic. The advantage of single-rail logic is that there is no active power consumption when it transfers data. It is better to design an encoding converter which has small overhead. Single-rail to dual-rail encoding converter which just uses a single NOT gate. Dual-rail to single-rail encoding Converter is unnecessary because the truth part of dual-rail encoding is same to single-rail encoding.

## 6. POSITIVE FEEDBACK ADIABATIC LOGIC

PFAL is new adiabatic technique which utilizes positive feedback. This logic structure consists of cross-coupled inverters, with NMOS devices are

connected between the outputs and the power-clock. In PFAL, sinusoidal power supply is used, known as power clock which is divided into four phases. In evaluate interval, the outputs are evaluated from stable input signal. During hold interval, output are kept stable, next is the recover interval, which recover the energy and the last is wait interval, inserted for the symmetry. PFAL is a dual-rail circuit which accept complementary inputs with respect to each other and provide outputs complemented with each other with partial energy recovery. The general schematic of the PFAL gate is shown in Fig1. Consist of an adiabatic amplifier, a latch made by the two PMOS and two NMOS, output nodes out and out B without any degradation in logic level. The functional blocks are in parallel with the PMOSFET of the adiabatic amplifier and form a transmission gate. The two n-trees realize the logic functions.

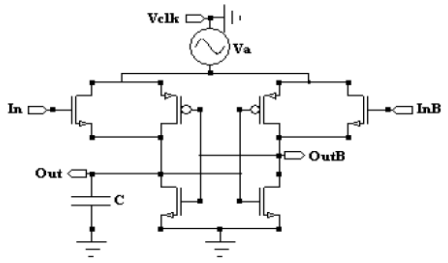


**Figure 1: PFAL Logic Circuit**

Power dissipation reduction is an important issue which needs to be focused for latest demand of technology. Dynamic power dissipation occurs in charging and discharging of capacitive loads. During charging current flows from Vdd to capacitive loads while in discharging, current flows from capacitive load to ground. Total charge transferred during charging/discharging cycle: Q = CL Vdd .Thus, an energy of E= $CLVdd^2$ is drawn from the power supply during charging. By assuming that the energy taken equals the energy supplied to the load capacitor, the energy stored into the load CL is half of the supplied energy: Estored = ( 1/2 )$CL\ Vdd^2$. The other half is dissipated in R. The same amount of energy is dissipated during the discharge process.

Adiabatic technique is used to increase energy efficiency of logic circuit in thermodynamic. For energy recovery circuit, the ideal energy dissipation when a capacitance C is charged from 0 to Vdd or discharged from Vdd, through a circuit of resistance R during time T is given by E= (RCS/T) $Vdd^2$. When T >> RC, the power consumption is much smaller. Q is the charge transferred to the load, C is the value of the load capacitance, R is the on-resistance of the PMOS switch, V is the final value of the voltage at the load, and T is the charging time. Adiabatic charging may be achieved by charging the capacitor from a time varying source that starts at Vi= 0V. This requires sinusoidal power supply. Theoretically, it is possible to reduce the power dissipation by extending the switching time. In this paper we are introducing ultra-low power comparator which is designed with different adiabatic technique.

### 6.1 Multiplexer Using PFAL Logic:

The proposed design of multiplexer is based upon adiabatic logic, in proposed design PFAL logic is used which is made from two PMOS and two NMOS that avoids the degradation of the logic level at the outputs. These NMOS devices are connected between output node and ground. A sinusoidal supply is applied. This logic family also generates both positive and negative outputs. The functional blocks are in parallel with the PMOS of the adiabatic amplifier and form a transmission gate. The two n- trees realize the logic functions. This logic family also generates both positive and negative outputs. The proposed multiplexer contains two modules: (i) a adiabatic multiplexer (ii) an XOR gate based on adiabatic logic. A multiplexer is designed using PFAL logic, it contains two inputs A, B one select line S and outputs out and out bar. A sinusoidal power clock is applied Vpc. When input is low, the output terminal „out" follow the sinusoidal power clock.

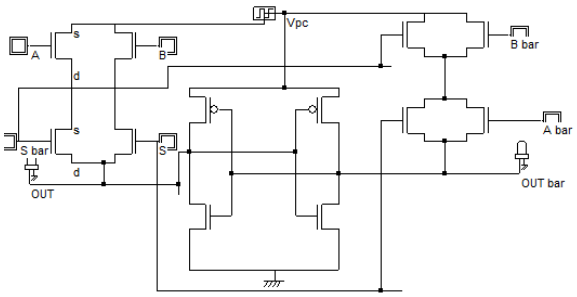


**Figure 2: Multiplexer Using PFAL Logic**

A two input XOR gate is designed using PFAL

logic, it contains two inputs A and B and the minimum sized XOR gate is implemented at 0.12ìm technology. Circuit shown has complementary outputs. One is X-OR and other is X-NOR. 2 PMOS and 10 NMOS are used in this design, width of the PMOS is kept 2 times larger than the NMOS in order to get equal rise and fall times as mobility of electron is 2-3 times larger than holes.

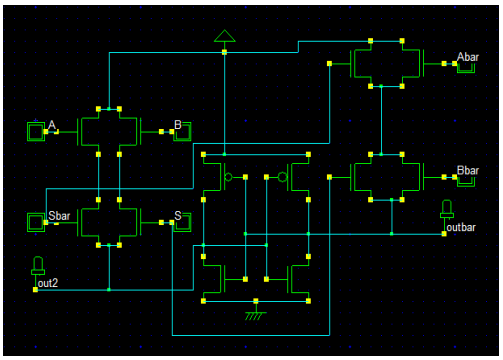


**Figure 3: Design of XOR Gate Using PFAL**

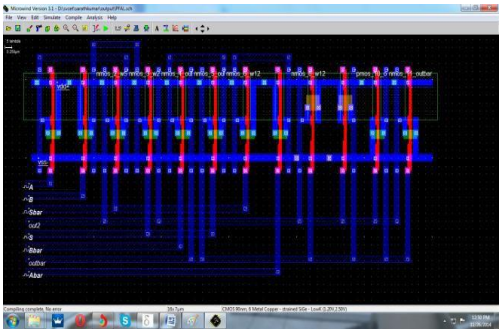

**Figure 4: Output for Stick Diagram**

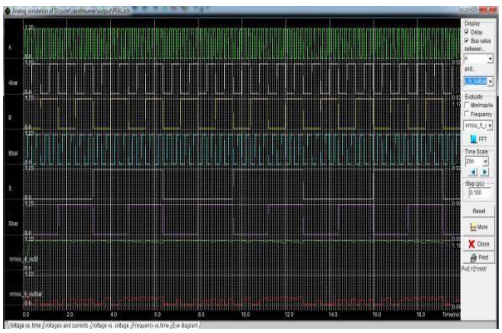

**Figure 5: Simulation Output**

## 7. CONCLUSION:

PFAL is designed using proposed adiabatic multiplexer which is designed with the help of four X-OR gate and two multiplexers. The proposed multiplexer is implemented using positive feedback adiabatic logic that saves power by recylcling the energy stored on load capacitor. This MULTIPLEXER USING PFAL is simulated at .12ìm technology. The proposed adiabatic multipexer saves 54.9% power at 1.2V than conventional CMOS based multiplexer design. It has been observed that proposed multiplexer saves 38.9% energy as compare to CMOS multiplexer. All results are verified at different supply voltage and temperature. Proposed Multiplexer USINGPFAL LOGIC RESULT good performance.

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