STUCK AT FAULT TESTING USING REVERSIBLE SEQUENTIAL CIRCUITS

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Abstract: we propose the design of two vectors testable sequential circuits based on conservative logic gates. Any sequential circuit based on conservative logic gates can be tested for classical unidirectional stuck-at faults using only two test vectors. The two test vectors are all 1s, and all 0s. The designs of two vectors testable latches, master-slave flip-flops and double edge triggered (DET) flip-flops are presented. The importance of the proposed work lies in the fact that it provides the design of reversible sequential circuits completely testable for any stuck-at fault by only two test vectors, thereby eliminating the need for any type of scan-path access to internal memory cells.

Intex Terms: Conservative logic, Fredkin gate, Flip-flops, Reversible logic.

1. INTRODUCTION

Conservative logic is a logic family that exhibits the property that there are an equal number of 1s in the outputs as there are in the inputs. Conservative logic can be reversible in nature or may not be reversible in nature. Reversibility is the property of circuits in which there is one- to-one mapping between the inputs and the output vectors that is for each input vector there is a unique output vector and vice-versa. Conservative logic is called reversible conservative logic when there is a one-to-one mapping between the inputs and the outputs vectors along with the property that there is equal number of 1s in the outputs as in the inputs. Conserv-ative logic circuits are not reversible, if one-to-one mapping between the inputs and the outputs vectors is not preserved.

We propose the design of testable sequential circuits based on conservative logic gates. The proposed technique will take care of the fan-out (FO) at the output of the reversible latches and can also disrupt the feedback to make them suitable for testing by only two test vectors, all 0s and all 1s. In other words, circuits will have feedback while executing in the normal mode. However, in order to detect faults in the test mode, our proposed technique will disrupt feedback to make conservative reversible latches testable as combinational circuits. The proposed technique is extended toward the design of two vectors testable master-slave flip- flops and double edge triggered (DET) flip-flops. Here simulation implementation using modelsim and Xilinx tools.

A conservative logic gate is a multiple-output logic element in which the number of 1s at the inputs is equal to that of the corresponding outputs. According to and a conservative logic circuit can be considered as a directed graph whose nodes are conservative logic gates, and the edges are wires of arbitrary lengths. The FO at the output is not allowed in conservative logic circuits. A conservative logic network can be reversible in nature if the one-to-one mapping is maintained between the inputs and the outputs, while it will be irreversible in nature if one-to-one mapping is not preserved. Any stuck-at-1 fault in the conservative logic circuit can be detected by setting all inputs to 0s followed by subsequent checking of the outputs for the presence of any 1s. Any stuck-at-0 faults can be detected by setting all inputs to 1s followed by subsequent checking of outputs for the presence of any 0s.

2. BACKGROUND

A conservative logic gate is a multiple-output logic element in which the number of 1s at the inputs is equal to that of the corresponding outputs. According to [7] and [8], The FO at the output is not allowed in conservative logic circuits. A conservative logic network can be reversible in nature if the one-to-one mapping is maintained between the inputs and the outputs, while it will be irreversible in nature if one-to-one mapping is not preserved. Researchers in [7], [9], and [10] have proved that: 1) in the event of unidirectional stuck-at-faults in a conservative logic network, either the number of 1s in its output set will differ from the number of 1s in its input set, or the output set is correct and 2) in a conservative logic network the two vector test sets, all 1s and all 0s,

provide 100% coverage for unidirectional stuck-at faults. Any stuck-at-1 fault in the conservative logic circuit can be detected by setting all inputs to 0s followed by subsequent checking of the outputs for the presence of any 1s. Any stuck-at-0 faults can be detected by setting all inputs to 1s followed by subsequent checking of outputs for the presence of any 0s. The comprehensive proofs can be referred in [7], [9], and [10].

A. Conservative Reversible Fredkin Gate

The Fredkin gate is a popularly used reversible conservative logic gate, first proposed by Fredkin and Toffoli in [8]. The Fredkin gate shown in Fig. 1 can be described as a mapping (A, B, C) to (P = A, Q = A⁻ B + AC, R = AB + A ⁻C), where A, B, C are the inputs and P, Q, R are the outputs, respectively.

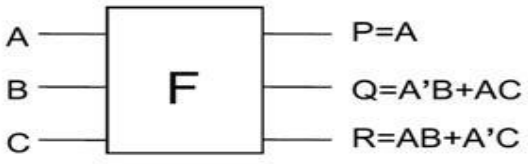

Fig- 1: Conservative Reversible Fredkin Gate

Table 1: Truth table of Fredkin Gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

The truth table for the Fredkin gate is illustrated in [3], which demonstrates that Fredkin gate is reversible and conservative in nature, that is, it has unique input and output mapping and also has the same number of 1s in the outputs as in the inputs.

B. Related Work

Any nanotechnology having applications of reversible logic, such as based on nano-CMOS devices, NMR-based quantum computing, or low power molecular QCA computing, all are susceptible to high error rates due to transient faults. With respect to this paper on reversible sequential circuits, the design of reversible sequential circuits is addressed in the various interesting contribution in which the designs are optimized in terms of various parameters, such as the number of reversible gates, garbage outputs, quantum cost, delay etc [11]–[13]. To the best of our knowledge, the offline testing of faults in reversible sequential circuits is not addressed in the literature.

3. DESIGN OF TESTABLEREVERSIBLE LATCHES

The characteristic equation of the D latch can be written as Q+ = D ■ E + E ■ Q. In the proposed work, enable (E) refers to the clock and is used interchangeably in place of clock .When the enable signal (clock) is 1, the value of the input D is reflected at the output that is Q^+ = D. when E = 0 the latch maintains its previous state, that is Q^+ = Q. The reversible Fredkin gate has two of its outputs working as 2:1 MUxes, thus the characteristic equation of the D latch can be mapped to the Fredkin gate (F). Fig. 3(a) shows the realization of the reversible D latch using the Fredkin gate. But FO is not allowed in conservative reversible logic. Moreover, the design cannot be tested by two input vectors all 0s and all 1s because of feedback, as the output Q would latch 1 when the inputs are toggled from all 1s to all 0s and could be misinterpreted as stuck-at-1 fault. The design has two control signals, C1 and C2.

The design can work in two modes:

Normal Mode: The normal mode is shown in Fig. 3(c) in which we will have C1C2 = 01 and we will have the design working as a D latch without any fan-out problem.

Test Mode (Disrupt the Feedback): In test mode, when C1C2 = 00 as shown in Fig. 3(d) it will make the design testable with all 0s input vectors as output T1

will become 0 resulting in making it testable with all 0s input vectors.

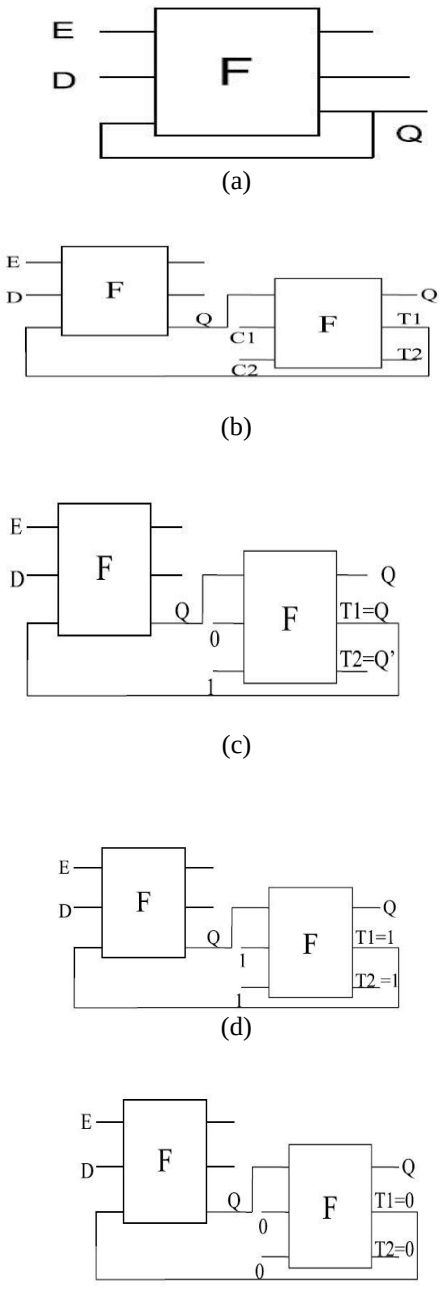

Figure 3: Design of testable reversible D latch using conservative Fredkin gate.

Fredkin gate based D latch. (b) Fredkin gate based D latch with control signals C1 and C2. (c) Fredkin gate based D Latch in normal mode: C1 = 0 and C2 = 1. (d) Fredkin gate based D latch in test mode for stuck-at-0 fault: C1 = 1 and C2 = 1. (e) Fredkin gate based D latch in test mode for stuck-at-1 fault: C1 = 0 and C2 = 0.

When C1C2 = 11 as shown in Fig. 3(e), the output T1, will become 1 and the design will become testable with all 1s input vectors for any stuck-at-0 fault. It can see from above that C1 and C2 will disrupt the feedback in test mode, and in normal mode will take care of the fan-out. Thus, our proposed design works as a reversible D latch and can be tested with only two test vectors, all 0s and all 1s, for any stuck-at fault by utilizing the inherent property of conservative reversible logic.

A. Design of Testable Negative Enable Reversible D Latch

A negative enable reversible D latch will pass the input D to the output Q when E = 0; otherwise maintains the same state. The characteristic equation of the negative enable D latch is

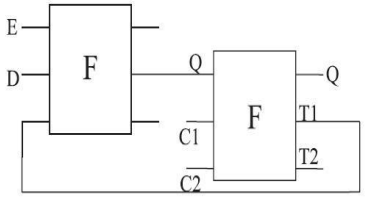

Figure 4: Fredkin gate-based negative enable testable D latch

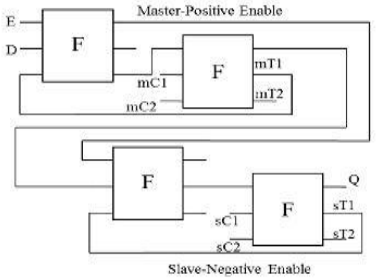

Figure 5: Fredkin gate-based testable reversible master-slave D flip-flop.

The characteristic equation of the D latch can be written as Q+ = D ■ E + E ■ Q. In the proposed work, enable (E) refers to the clock and is used interchangeably in place of clock. The negative enable D-latch of the Fredkin gate as shown in Fig. 4. The second Fredkin gate in the design take cares of the FO. The second Fredkin gate in the design also helps in making the design testable by two test vectors, all 0s

and all 1s, by breaking the feedback based on control signals C1 and C2 as illustrated above for positive enable reversible D latch.

4. DESIGN OF TESTABLE MASTER-SLAVE FLIP-FLOPS

In the existing literature, the master-slave strategy of using one latch as a master and the other latch as a slave is used to design the reversible flip-flops [13]. In this paper, we have proposed the design of testable flip-flops using the master-slave strategy that can be tested for any stuck-at faults using only two test vectors, all 0s and all 1s. Fig. 5 shows the design of the master-slave D flip-flop in which we have used positive enable Fredkin gate-based testable D latch shown in Fig. 3(b) as the master latch, while the slave latch is designed from the negative enable Fredkin gate-based testable D latch shown earlier in Fig.4.The testable reversible D flip-flops has four control signals mC1, mC2, sC1, and sC2. mC1 and mC2 control the modes for the master latch, while sC1 and sC2 control the modes for the slave latch. In the normal mode, when the design is working as a master-slave flip-flop the values of the controls signals will be mC1 = 0 and mC2 = 1, sC1 = 0 and sC2 = 1.

5. DESIGN OF TESTABLE REVERSIBLE DET FLIP-FLOPS

The DET flip-flop is a computing circuit that samples and stores the input data at both the edges, which is at both the rising and the falling edge of the clock. The master-slave strategy is the most popular way of designing the flip flop. In the proposed work, E refers to the clock and is used interchangeably in place of clock. In the negative edge triggered master-slave flip-flop when E = 1 (the clock is high), the master latch passes the input data while the slave latch maintains the previous state. When E = 0 (the clock is low), the master latch is in the storage state while the slave latch passes the output of the master latch to its output. Thus, the flip-flop does not sample the data at both the clock levels and waits for the next rising edge of the clock to latch the data at the master latch.

In order to overcome the above problem, researchers have introduced the concept of DET flip-flops, which sample the data at both the edges. Thus, DET flip-flops can receive and sample two data values in a clock period thus frequency of the clock can be reduced to half of the master-slave flip flop while maintaining the same data rate.. The DET flip-flop is designed by connecting the two latches, viz., the positive enable and the negative enable in parallel rather than in series. The 2:1 MUX at the output transfer the output from one of these latches which is in the storage state (is holding its previous state). The conventional design of the DET flip-flop can be found in [15]. The equivalent testable reversible design of the DET flip flop is proposed in this paper and is shown in Fig. 6.

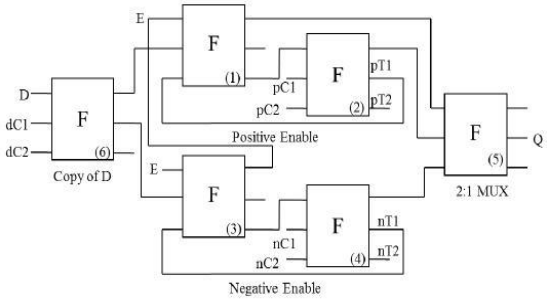

Figure 6: Fredkin gate-based DET flip-flop

Normal Mode: The normal mode of the DET flip-flop is illustrated in Fig. 6(b) in which the pC1 = 0, pC2 = 1, nC1 = 0, and nC2 = 1. The pC1 = 0, pC2 = 1 help in copying the output of the positive enable D latch thus avoiding the FO while the nC1 = 0 and nC2 = 1 help in copying the output of the negative enable D latch thus avoiding the FO.

Test Mode: There will be two test modes.

All 1s Test Vectors: This mode is control signals will have value as pC1 = 1, pC2 = 1, nC1 = 1, and nC2 = 1. This makes the design testable by all 1s test vector for any stuck-at-0 fault. (Breaking the feedback of the negative enable D latch)

All 0s Test Vectors: This mode is the control signals will have value as pC1 = 0, pC2 = 0, nC1 = 0, and nC2 = 0. The pC1 = 0 and pC2 = 0 this makes the design testable by all 0s test vector for any stuck-at-1 fault. (Breaking the feedback of the negative enable D latch.)

6. CONCLUSION

This proposed reversible sequential circuits based on conservative logic that is testable for any unidirectional stuck-at faults using only two test vectors, all 0s and all 1s. Hence, a conventional sequential circuit needs modification in the original circuitry to provide the

testing capability.Thus, the main advantage of the proposed conservative reversible sequential circuits compared to the conventional sequential circuit is the need of only two test vectors to test any sequential circuit irrespective of its complexity. The reduction in number of test vectors minimizes the overhead of test time for a reversible sequential circuit.

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