A STUDY ON SPECIFIC COMPUTATION METHODS IN VLSI PHYSICAL DESIGN

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Abstract: The rapid development of the VLSI industry is unable to keep up with the demands created by the growth of device capacity and expansion of the user population. There is a need to produce a placement solution that can address high quality placement within a shorter time. Additionally, faster placement and routing tools are required to handle complicated tasks. The objective of the research work was to obtain maximum speed and minimum interconnection of the partitioning problem with the help of Markovian models. The unimodular hyper graph has been proposed as an alternative approach to ne tlist with the help of transition probability matrices. Further, uni modular hyper graph is utilized to maximize flow at a particular node and minimize the time between two nodes. In order to address the clustering challenges, this study confirms that K-medoid method overcame VLSI partitioning problem by using medoids to represent the cluster rather than centroid. Two novel methods have been introduced to analyze the Markov Renewal Reward method for VLSI circuit partitioning. Another important contribution of this study is to employ utility theory under risk and uncertainty, and to solve cell placement problem.

Keywords: VLSI, Unimodular Hyper Graph, two-step clustering, hierarchical clustering, K-medoids clustering, Markov Renewal Reward process

1. INTRODUCTION

Generally, very large scale integration (VLSI) comprises an excess of over one million transistors. Yet, the term 'VLSI' still remains to be accepted and denotes digital integrated systems with high complexity. The computer-aided design (CAD) has further aided the growth in the complexity and performance of integrated circuits in the VLSI technology. Thus, it is crucial to manage the design process to maintain the reliability, quality, and extensibility of a given design. The process includes "definition, execution and control of design methodologies in a flexible and configurable way" [1], [2]. Speed of development in high-performance computing, telecommunications and consumer electronics in a rapidly changing market, developmental costs, and cost involved in case of mistakes play a critical role in a commercial environment [3]. Hence, it requires designs that can be processed quickly, cheaply and mistakes realized at the earliest.

VLSI is preferred due to its compactness, less occupancy of space, higher speed, lower parasitic length, lower power consumption, higher reliability and improved on-chip interconnects. Additionally, VLSI integration significantly reduces manufacturing cost.

Nevertheless, a few disadvantages, such as long design and fabrication time and higher risk to project with complexity of millions of components leads to the anticipation of fast computation and layouts close to optimality generation. The research and development of circuit layout automation tools could pave a way for future growth of VLSI systems.

Problems arising as a result of optimization need to be solved during the circuit layout, which is intractable [4], [5]. This refers to the fact that they are mostly Nondeterministic Polynomial (NP)-hard [6]. The major implication of this recourse is that the optimal solutions cannot be achieved in polynomial time.

The present study addresses the following gaps:

- The growth of device capacity and the expansion of a new user population have resulted in new challenges on CAD software for VLSI design.
- A need to achieve scalability across the entire flow through CAD software for VLSI, without much sacrifice on the quality of the result.
- A need to produce an efficient placement solution which can address high quality placement within a shorter time.
- Faster placement and routing tools are required to handle complicated tasks. They should be flexible and robust to handle any modifications in VLSI design styles and design objectives.

The aim of this study is to develop and examine new methods and strategies, which are robust and flexible to perform the partitioning and placement tasks.

The main objectives of this study are

- To introduce a special type of hyper graph called unimodular hyper graph.
- To address the various clustering methods used to obtain effective VLSI circuit partitioning.
- To investigate an alternative method, namely Markov Renewal Reward process for VLSI circuit partitioning, which is a stochastic process under continuous time and discrete values?
- To address circuit placement challenges through utility theory

2. UNIMODULAR HYPERGRAPH

The unimodular hyper graph and the partitioning problem are defined with special emphasis on matrices and logic circuits. The qualifications required for hyper graph to be unimodular hyper graphs are discussed along with the application of unimodular hyper graphs for obtaining the maximum flow at a particular node and for minimizing the time between two nodes. A variety of partitioning techniques ranging from multilevel methods to advanced search heuristics to mathematical programming methods are explained in this study [7].

3. CLUSTERING APPROACHES

The existing approaches to the graph and hyper graph partitioning problems are discussed. Since graph and hyper graph partitioning are NP-complete problems, this study considers the need for developing various clustering models that yield good sub-optimal solutions. A different clustering approach to solve VLSI circuit partitioning problem has been proposed as a solution to this problem. Useful sub-circuits with the lowest amount of interconnection were studied to bridge the gap. Three different data clustering methods namely two-step clustering, hierarchical clustering and K-medoids clustering were considered in dividing the circuits into sub-circuits.

The main objective of the study is to compare the K-medoids clustering with two-step and hierarchical clustering. The results were analyzed based on the size of the data set and run time factor of each of the algorithms. K-medoid clustering takes less execution time and more data coverage. Hence, this study proves that K-medoid clustering achieves greater performance in comparison to two-step and hierarchical clustering.

4. MARKOV CHAIN MODELS

The benefits of Markov chain model are described and the Markov renewal reward process is investigated in this study. The extension of the Markov renewal theorem is described for analyzing more complex queuing system or reliability. An attempt is made to investigate the probability distribution of the accumulated reward in a Markov renewal process and to obtain the accumulated reward that is directly influenced by a random process that can be modeled by continuous-time Markov chain. In doing so, two novel approaches were employed and described along with the strategies in this study [8],[9].

The main focus of this study is on determining the optimal criterion for the total expected discounted cost as it is found to be more appropriate and essential. Alternatively, one can concentrate on a long-run average cost per unit time.

5. UTILITY THEORY

An attempt has been made to focus on the notion of utility theory in both decision making under risk and uncertainty. Additionally, the efficiency of the selection of three types of utility curves, such as Conservation Man, Average player and the Gambler has been investigated. Further, the utility theory has been analyzed for its efficiency to solve cell placement problem [10].

6. CONCLUSION

VLSI research has witnessed an enormous increase in the past few decades to address the challenges faced in the rapidly changing market of high-performance computing, telecommunications and consumer electronics. Developmental costs and the cost involved in case of any mistakes play a critical role in a commercial environment of these technologies. With such great stakes involved and a phenomenal increase in complexity, it is more crucial than ever before to manage the design process and to maintain the reliability, quality, and extensibility of a given design. Therefore, an attempt was made in this study to develop

and examine new methods and strategies that are robust, flexible, and efficient to perform the partitioning and placement tasks. The basic techniques proposed in this thesis can be extended to enhance their functionality and performance. The following are several possibilities that can be investigated for extending these basic techniques.

- Reducing delay in the placement phase in clustering models.
- Constructing scalable parallel partitioning algorithm for two-dimensional distributions in VLSI cell placement.
- Improving placement efficiency by utilizing a technique of Markov renewal reward process.
- Examining utility theory for tackling the challenges in VLSI physical design problem such as cell routing.
- Investigating Decision Making Theory and Game Theory for solving issues in VLSI physical design.
- Examining and including models to estimate problems associated with wires in a channel such as congestion and cross talk.

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