PERFORMANCE ANALYSIS OF DUAL GATE MOSFET IN PARALLEL ADDER

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Abstract: This paper describes a parallel single-rail self-timed adder using dual gate MOSFETs which builds on a recursive formulation for performing multibit binary addition. Thus the addition is equivalent for those bits that do not need any carry chain propagation and the circuit attains logarithmic performance over random operand conditions without any special speedup circuitry or look-ahead schema. A real design of dual gate MOSFET is provided along with a completion finding unit. The design is regular and does not need any real limitations of high fan outs. A high fan-in gate is necessary on the design but this is unavoidable for asynchronous logic and is managed by connecting the transistors in parallel. Simulations have been executed using LT spice tool that verify the practicality and superiority of the proposed approach over existing asynchronous adders.

Index terms: Asynchronous circuits, DGMOSFET design, binary adders, digital arithmetic.

1. INTRODUCTION

Binary addition is the most important operations that a processor performs. Most of the adders have been designed using synchronous circuits even though there is a strong interest in clock less or asynchronous processors/circuits. Asynchronous designs are those which do not accept any quantization of time. Therefore, they support a great potential for logic design as they are free from many problems from clocked (synchronous) circuits. In common, logic flow in asynchronous circuits is coordinated by a request-acknowledgment handshaking Protocol signals to create a pipeline in the absence of clocks. Explicit handshaking blocks are minor elements, such as bit adders, are costly. Therefore, it is implicitly and successfully achieved using dual-rail carry propagation in adders. A legal dual-rail carry output also provides an acknowledgment signal from a single-bit adder block. Thus, asynchronous adders are built on either full dual-rail encoding of all signals (more formally using null convention logic that uses symbolically correct logic as an alternative of Boolean logic) or pipelined process using single-rail data encoding and dual-rail carry sign for response signals. While this creates add robustness to circuit designs and they also bring together significant overhead to the average case performance on asynchronous adders add benefits. Therefore capable alternative approach that can address these problem presents an asynchronous parallel self-timed adder (PASTA) using the algorithm first proposed. The design of PASTA using dual gate MOSFET is regular and uses half-adders (HAs) along with multiplexers have need of minimal interconnections. Thus, it is suitable for completion of VLSI circuits. The design works in a parallel manner which is unique as it employs feedback through XOR logic gates to create a single-rail cyclic asynchronous sequential adder. Cyclic circuits can be added efficient on resource than their acyclic counterparts. The another way that wave pipelining (or maximal rate pipelining) is a method that can apply pipelined inputs before the stabilization of outputs. The proposed circuit succeeds automatic single-rail pipelining of the carry inputs which is distinguished by propagation and inertial delays of the gates in the circuit path. Thus a single rail wave-pipelined method is effective and quite varied from conventional pipelined adders using dual-rail encoding to implicitly represent the pipelining of carry signals independent carry chain blocks.

2. PARALLEL ADDERS

Parallel adders are considered to be a combinatorial circuit which is not clocked, does not have any memory and feedback circuit elements for adding every bit position of the operands in the same time. Fig 1 shows the parallel adder thus it have need of number of bit-adders which consists of (full adders + 1 half adder) equal to the number of bits to be added.

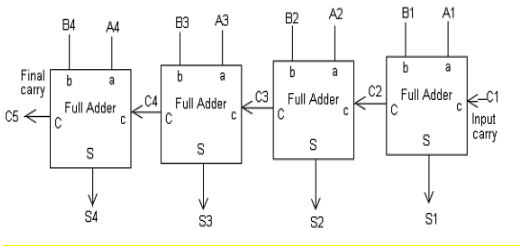

Figure 1: Parallel adders

3. SELF TIMED CIRCUITS

An asynchronous circuits are similarly called self-timed circuit, is a sequential digital logic design which is not controlled by a clock circuit or global clock signal. As an alternative they always use signals that show completion of instructions and operations stated by simple data transfer protocols. This type is different from synchronous circuit in which variations to the signal values in the circuit are activated by repetitive pulses called a clock signal. However asynchronous circuits have the possible to be faster, and may also have other advantages in minor power consumption, lower electromagnetic interference, and well modularity in large a system which has active area of research in design. In asynchronous circuits, there is nonappearance of clock and the state of the circuit changes as soon as the input changes. Since they don't have to pause for a clock pulse to begin process of the inputs, asynchronous circuits can be quicker than synchronous circuits, and their speed is theoretically restricted only by the propagation delays of the logic gates. In principle, the asynchronous systems has the possible advantages over synchronous systems: (i) lower power, since an asynchronous component work out only when it is necessary; (ii) higher act, since global clock distribution and synchronization can be prevented and finally, (iii)greater modularity and comfort of design, since there are no global timing constraints in the design.

There are myriad projects of binary adders and here on asynchronous self-timed adders. Self-timed defines a logic circuits that can be governed by and/or engineer timing idea for the accurate operation. Self-timed adders have the possible to run faster be close to the dynamic data, as early completion detecting can avoid the need for the worst case bundled delay mechanism of synchronous circuits.

3.1 Pipelined Adders Using Single-Rail Data Encoding

The asynchronous Req/Ack handshake can be used to pass the adder block as well as to create the flow of carry signals over the design. In utmost of the cases, a dual-rail carry resolution is attained for internal bitwise flow of carry outputs. These dual-rail signals can denote more than two logic values (invalid, 0, 1), and that can be used to provide bit-level reply when a bit operation is completed. Final completion is sensed using all bit Ack signals are received at high. The carry-completion detecting adder is an example of a pipelined adder, which uses full adder (FA) functional blocks adjusted for dual-rail carry. On the other hand, a predictable completion adder circuit is intended. It also called terminate logic and early completion to select the same completion response from a number of fixed delay lines. However, the dismiss logic implementation is costly due to the necessary of high fan-in requirements.

3.2 Delay Insensitive Adders Using Dual-Rail Encoding

Delay insensitive (DI) adders are also asynchronous adders that state bundling controls or DI operations. Therefore, they can properly operate in the presence of bounded but unknown gate and wire delays. There are various DI adders, such as DI ripple carry adder (DIRCA) and DI carry look-ahead adder (DICLA). DI adders use dual-rail encoding and are estimated to increase complication. Though a dual-rail encoding doubles the wire difficulty, they can still be used to yield circuits nearly as effective as that of the single-rail variants using dynamic logic or nMOS only designs. As similar to 40 transistors per bit DIRCA adder is designed in while the conservative CMOS RCA uses 28 transistors. Similar to CLA, the DICLA has carry propagate, generate, and destroys equations in terms of dual-rail encoding. They do not connect to the carry signals in a chain but arrange them in a categorized tree. Thus, they can be originally operate faster when there is long carry chain. Fig 2 shows the general block diagram of PASTA.

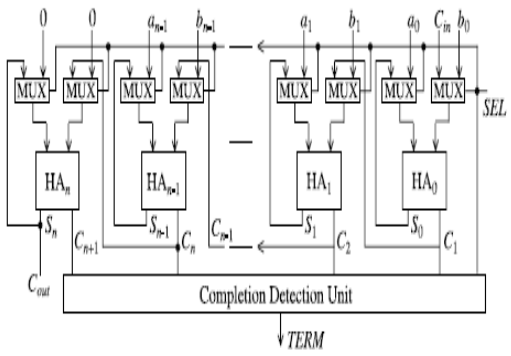

Figure 2: General block diagram of PASTA

A further optimization is obtained from the shows that dual rail encoding logic can benefit from settling of either the 0 or 1 path. Dual-rail logic need not pause for two paths to be evaluated. Thus, it is achievable to additional speed up the carry look-ahead circuitry to send the carry-generate/carry-kill signals to any level in the tree. This is defined and referred as DICLA with speedup circuitry (DICLASP).

4. EXISTING SYSTEM

Fig 3 shows the adder first receives two input operands to perform half additions for each bit. Successively it iterate on using earlier generated carry and sums to perform half-additions repetitively until all carry bits are consumed and settled at zero level and complete the process.

4.1 Parallel Self Timed Adder

The selection of input for two-input multiplexers resembles to the Req handshake signal and will be a single 0 to 1 transition symbolized by SEL. It will primarily select the actual operands during SEL = 0 and also switch to feedback/carry paths for successive iterations using SEL = 1. The feedback path from the half adders allows the multiple iterations to continue until the completion when all carry signals will accepts zero values.

4.2 State Diagram

Each state is denoted by a ($C_{i+1}S_i$) pair where $C_{i+1}S_i$ represent carry out and sum values correspondingly from the i_{th} bit adder block. Fig 3 displays the two state diagrams are drawn for the initial phase and the iterative phase of the designed architecture. During the early phase the circuit simply works as a combinational HA processing in fundamental mode. It is actual that due to the use of half adders in its place of full adders state (11) cannot perform. During the iterative phase (SEL = 1), the feedback path over multiplexer block is stimulated using SEL. The carry transitions (C_i) are allowable as many times as needed to whole recursion.

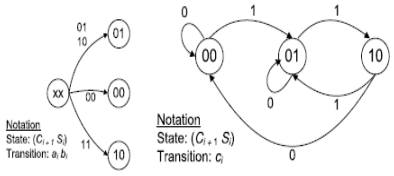

Figure 3: State diagrams for PASTA

a) Initial Phase b) Iteration phase

From the definition of fundamental mode circuits the present design cannot be calculated as a fundamental mode circuit as the input–outputs will go through several transitions before generating the final output. That it is not a Muller circuit working outside the fundamental mode both as internally several transitions will take place as shown in the state diagram. This is same to cyclic sequential circuit where gate delays are used to separate individual states.

4.3 Recursive Formula for Addition

Let S_{ji} and C_{ji+1} defines the sum and carry correspondingly for i_{th} bit at the j_{th} iteration. The early condition (j= 0) for addition is denoted by:

$$S_i^{\,0} = a_i \oplus b_i$$

$$C_{i+1}^{\,0} = a_i\, b_i \qquad (1)$$

The j_{th} iteration for the recursive adding is denoted by

$$S_i^{\,j} = S_i^{\,j-1} \oplus C_i^{\,j-1} \; 0 \le i < n \qquad (2)$$

$$C_{i+1}^{\,j} = S_i^{\,j-1} C_i^{\,j-1} \; 0 \le i \le n \qquad (3)$$

The recursion is aborted at k_{th} iteration when the following condition is met:

$$C_n^k + C_{n-1}^k + \cdots + C_1^k = 0, 0 \le k \le n. \quad (4)$$

4.5 Implementation

A CMOS performance for the recursive circuit shown in Fig 4..For multiplexers and AND gates using the TSMC library execution while for the XOR gate we have used the faster ten transistor execution based on transmission gate XOR to tie the delay with AND gates. The completion detection following is terminated to obtain an dynamic high completion signal (TERM). This involves a large fan-in n-input NOR gate. Therefore various more practical pseudo-nMOS ratioed design is used.

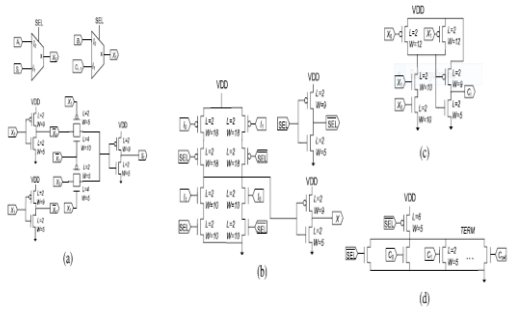

Figure 4: CMOS execution of PASTA

Using the pseudo-nMOS project the completion unit gets out of the high fan-in problem as all the connections are similar. The pMOS transistor connected to V_{DD} of these ratioed design performances as a load register concludes in static current drain when some of the nMOS transistors are on simultaneously. In addition to the C_i the negative of SEL signal is also take in for the TERM signal to promise that the completion cannot be accidentally turned on during the initial selection phase of the real inputs. It also avoids the pMOS pull up transistor from being always on.

Hence static current will only be flowing for the period of the real computation. VLSI layout has also been estimated for a standard cell environment using two metal layers. The layout space captures 270 λ × 130 λ for 1-bit resulting in 1.123 Mλ^2 area for 32-bit. The pulls down transistors of the completion detection logic are taken in the single-bit layout while the pull-up transistor is furthermore placed for the full 32-bit adder.

It is nearly twice over the area required for RCA and is fairly less than the most of the area efficient prefix tree Brent–Kung adder (BKA).The design works in a similar manner for independent carry chain blocks it is varied as it employs feedback through XOR logic gates to constitute a single-rail cyclic asynchronous sequential adder.

Cyclic circuits can be more resource effective than their acyclic equivalents. On the other words wave pipelining (or maximal rate pipelining) is a technique that can apply pipelined inputs earlier the outputs become stable. The proposed circuit attains automatic single-rail pipelining of the carry inputs separated by propagation and inertial delays of the gates in the circuit path. Thus it is efficiently a single rail wave-pipelined approach and quite varied from conventional pipelined adders using dual-rail encoding to implicitly represent the pipelining of carry signals.

5.PROPOSED SYSTEM

5.1 PASTA Design Using DGMOSFET

Multiplexers are design that selects one of several analog or digital input signals and forwards the selected input into a lone line. Multiplexers and AND gates are used by library executions while for the XOR gate it uses the faster ten transistor execution based on transmission gate XOR to tie the delay with AND gates. Memory-sharing fractional parallel architecture achieves a good balance on throughput and hardware cost in a large range. The measurement of critical path done which is equal for top and bottom leads to high clock frequency. Encoding is very useful to these LDPC codes for that reason the number of incoming messages to each processing units are uniform across the entire clock cycles.

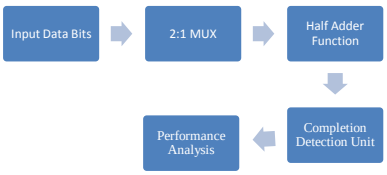

Figure 5: Block diagram of proposed system

Fig 5 displays the proposed block diagram of PASTA which has the performance analysis block to evaluate the performance of the circuit.

5.2 Dual Gate MOSFET

DGMOSFET consist of lightly doped ultra-thin layers seem to be a favorable option for ultimate scaling of CMOS technology. Outstanding short channel effect (SCE) immunity high trans conductance and ideal sub threshold factor have been providing by many theoretical and experimental studies on that device.

5.3 Structure of Dual Gate MOSFET

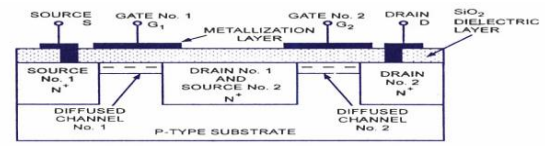

Figure 6: Dual gate MOSFET

The dual gate MOSFET is a form of MOSFET has two gates which are fabricated along the length of the channel one after another. In this way, both gates disturb the level of current flowing between the source and drain channel. DGMOSFET is consist of a conducting channel (usually undoped) bounded by gate electrodes on both side. This accepts that no part of the channel is far away from a gate electrode. In effect the dual gate MOSFET operation can be considered equivalent to the two MOSFET devices in series shown in Fig 6. Both gates will affect the overall performance of MOSFET operation and output. The dual gate MOSFET has referred as tetrode construction where the two grids control the current over the channel. The two different gates control various sections of the channel which are in series with each other.

5.4 Design Challenges

Control of VTT is denoted as the value of V_{gs} which is needed to obtain surface inversion creating a conducting channel. Due to scaling of V_{dd} we need to have very low (~0.2 V) and symmetrical (V_{Tn}= -V_{Tp}) threshold voltages for both transistor types. For DGMOSFETs, V_T is initially controlled by φ gate. With a unique mid gap material for both the NMOS and PMOS symmetrical V_T can be achieved but the value is too large (~0.8 V).

5.5 Fabrication Issues

Fabrication of the DGMOSFET is difficult. Alignment of both gates is hard to attain but it is needed for good device performance. A wrong aligned gates results in the extra capacitance and loss of current drive. Several different structures have been planned to deal with fabrication issues including planar and quasi-planar structures.

5.6 Advantages

Fall of I_{off}. Undoped channel removes intrinsic parameter fluctuations and controls impurity scattering. Double gate obtain for higher current drive capability and has better control of short channel effects.

5.7 Application

There are different applications of DGMOSFET in digital and in analog field such as reconfigurable gates which can achieve multiple operations, variable gain amplifiers, high frequency mixers etc.

6. RESULTS

LT spice is an analog circuit simulator with integrated schematic capture and waveform viewer in that tool. It was explicitly written to outperform analogous tools for sale from software companies in the demand of being used for in house IC design as part of Linear Technology Corporation's competitive advantage as a semiconductor company.

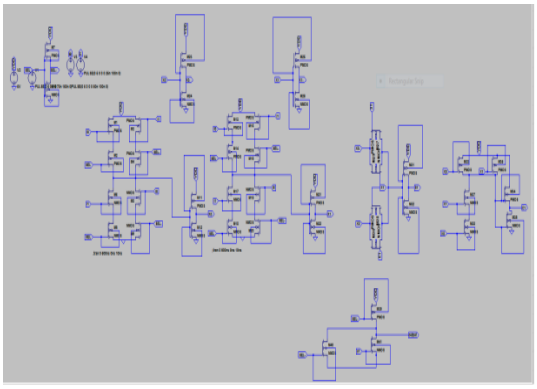

Figure 7: PASTA is designed using DGMOS

The Fig 7 displays the implementation of parallel self-timed adder using DGMOS.

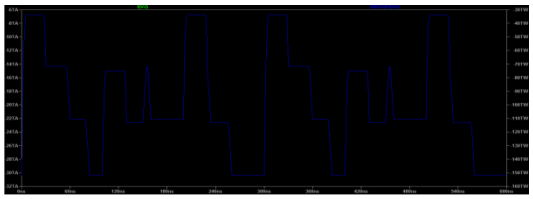

Figure 8: Average power consumption using DGMOS

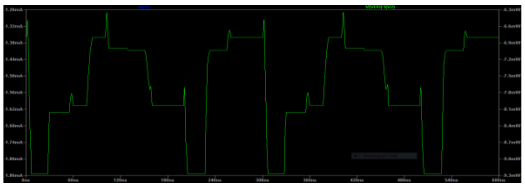

Figure 9: Average power consumption using CMOS

Thus the parallel self-timed adder is planned using DGMOS which has a improved performance over the CMOS. And the result shows thus the power consumption in the circuit is decreased while using dual gate MOSFETs.

7. CONCLUSION

This brief presents an effective implementation of a adder using DGMOSFET. Initially, the theoretical foundation for a single-rail wave-pipelined adder is designed. The design achieves a very simple n-bit adder that is area and interconnection-wise equals to the performance of simple adder namely the RCA. Thus the DGMOS circuit works in a similar manner for independent carry chains, and thus provides logarithmic average time performance over random input standards. The finishing point detection unit for the proposed adder using dual gate MOSFET is real and efficient. Simulation results are used to evaluate the advantages of the proposed design.

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