

DESIGN OF CONFIGURABLE MULTIPLIERS USING DUAL QUALITY 4:2 COMPRESSORS

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Abstract: Multiplier plays a vital role in many applications such as digital image processing, digital signal processing etc...so it is important to design the multiplier with low power consumption and reduced delay. In order to reduce this factor we design the multiplier using four 4:2 compressor and these compressors has a dual quality property and this property is used to switch between the exact and approximate modes. When it operates at approximate mode it reduces the power consumption and area at the cost of low accuracy. During approximate and exact mode each of these compressors has different power consumption and delays but only at approximate mode these compressors has its own level of accuracy. Hence these compressors are used in the design of parallel multiplier. These parallel multipliers provides configurable multiplication whose accuracy may change dynamically during the run time. We implement these compressors in a 32 bit data multiplier which is evaluated in a 45 nm standard CMOS technology.

Index Terms: Power, 4:2 compressors, Accuracy, Approximate computing, Configurable, Delay

1. INTRODUCTION

The most commonly used techniques for the generation of approximate arithmetic circuits are truncation, voltage over scaling (VOS) and simplification of logic. Extensive research has been conducted on approximate address providing significant gains in terms of area and power while exposing small error. Approximate hardware circuits, contrary to software approximations, offer transistors reduction, lower dynamic and leakage power, lower circuit delay, and opportunity for downsizing.

Motivated by the limited research on approximate multipliers, compared with the extensive research on approximate adders, and explicitly the lack of approximate techniques targeting the partial product generation, we introduce the partial product perforation method for creating approximate multipliers. We omit the generation of some partial products, thus reducing the number of partial products that have to be accumulated; we decrease the area, power, and depth of the accumulation tree. By reducing the quality (accuracy), the delay and/or power consumption of the unit may be reduced. In addition, some digital systems, such as general purpose processors, may be utilized for both approximate and exact computation modes [4]. An approach for achieving this feature is to use an approximate unit along with a corresponding correction unit. The correction unit, however, increases the delay, power, and area overhead of the circuit. Also, the error

correction procedure may require more than one clock cycle, which could, in turn, slow down the processing further

2. EXISTING SYSTEM

2.1 Compressor4:2:

This type of compressor, shown schematically in Fig.1. has four inputs (x1-x4) along with an input carry (Cin), and two outputs (sum and carry) along with an output Cout.

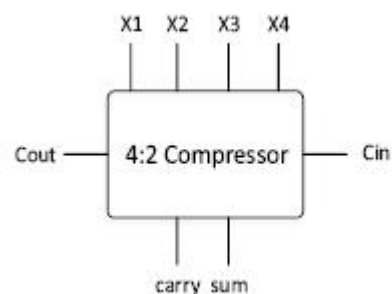


Figure 1: Block diagram of 4:2 compressor

The compressor 4:2 trees also has a regular structure and sums the partial products as a binary tree does, using 4:2 compressors instead of CSAs.

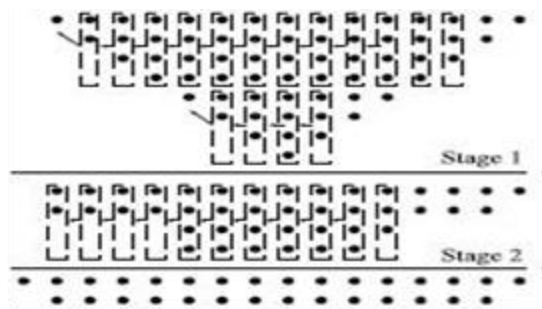


Figure 2: Dot diagram for an multiplier using exact 4:2 compressor

3. PROPOSED SYSTEM

In this paper, we present four dual-quality reconfigurable approximate 4:2 compressors, which provide the ability of switching between the exact and approximate operating modes during the runtime. The compressors may be utilized in the architectures of dynamic quality configurable parallel multipliers. The basic structures of the proposed compressors consist of two parts of approximate and supplementary. In the approximate mode, only the approximate part is active whereas in the exact operating mode, the supplementary part along with some components of the approximate part is invoked.

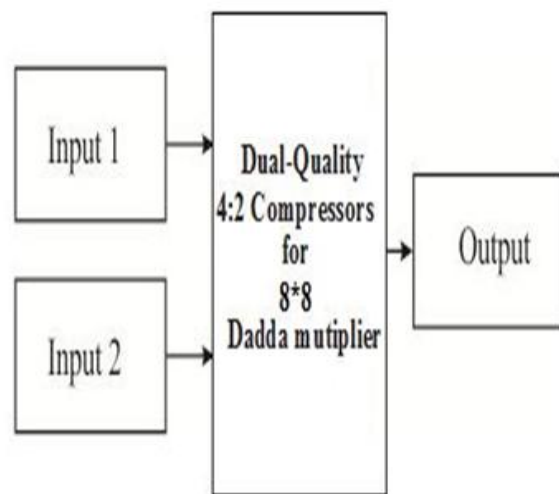


Figure 3: Block diagram of proposed system

The proposed DQ4:2Cs operate in two accuracy modes of approximate and exact. The general block diagram of the compressors.

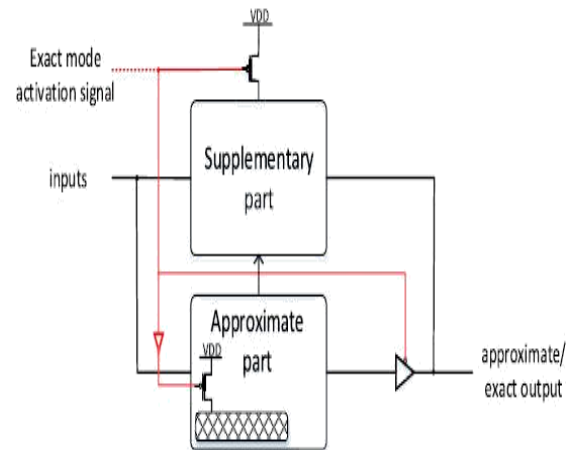


Figure 4: .Block diagram of proposed approximate 4:2 compressors. The hachured box in the approximate part indicates the components, which are not shared between this and supplementary parts

The diagram consists of two main parts of approximate and supplementary. During the approximate mode, only the approximate part is exploited while the supplementary part is power gated. During the exact operating mode, the supplementary and some parts of the approximate parts are utilized. In the proposed structure, to reduce the power consumption and area, most of the components of the approximate part are also used during the exact operating mode. We use the power gating technique to turn OFF the unused components of the approximate part.

3.1 Approximate part of DQ4:2C4:

The overall structure of DQ4:2C3 is shown in Fig.5. Where the supplementary part is enclosed in a red dashed line rectangle. Note that in this structure, the utilized NAND gate of the approximate part (denoted by a blue dotted line rectangle) is not used during the exact operating mode. Hence, during this operating mode, we suggest disconnecting supply voltage of this gate by using the power gating.

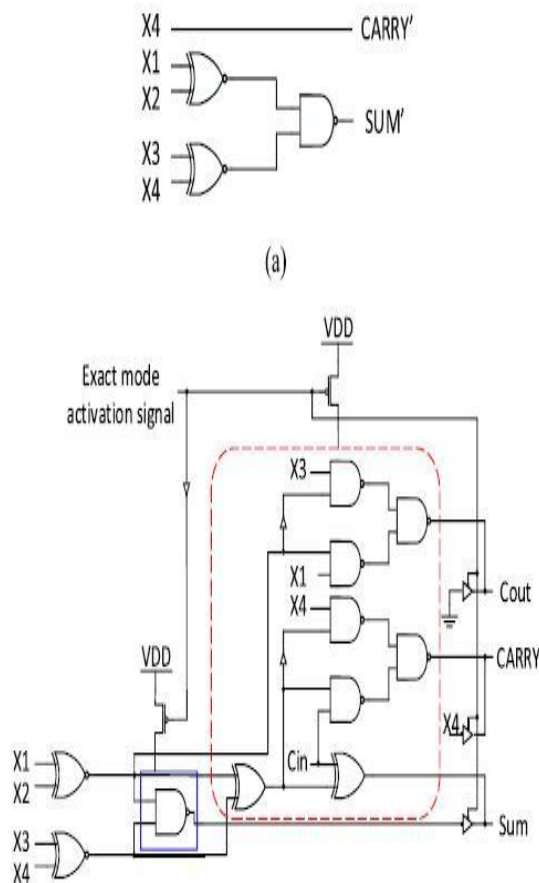


Figure 5: (a) Approximate part of DQ4:2C3 and (b) Overall structure of DQ4:2C3s

3.2 Overall structure of DQ4:2C4:

In this structure, we improve the accuracy of the output carry compared with that of DQ4:2C3 at the cost of larger delay and power consumption where the error rate is reduced to 31.25%. The internal structure of the approximate part and the overall structure of DQ4:2C4 are shown in Fig. The supplementary part is indicated by red dashed line rectangular while the gates of the approximate part, powered OFF during the exact operating mode, are indicated by the blue dotted line. Note that the error rate corresponds to the occurrence of the errors in the output for the complete range of the input.

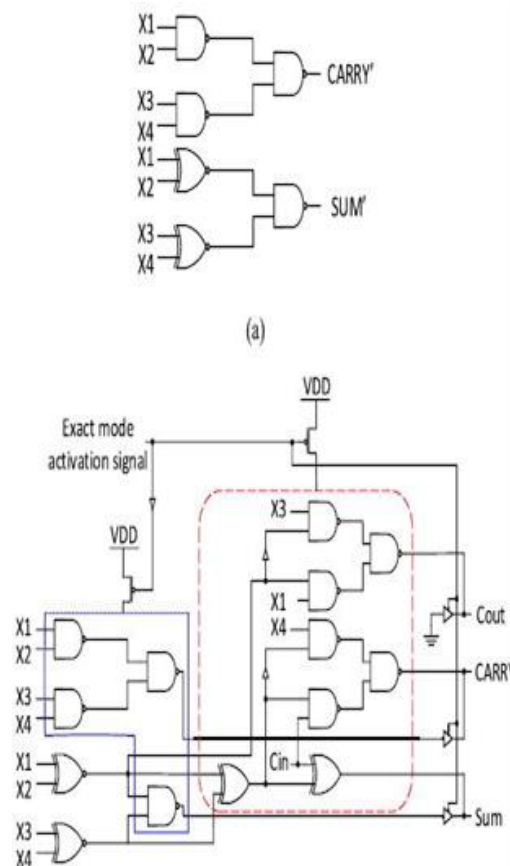


Figure 6: (a) Approximate part of DQ4:2C4 and (b) Overall structure of DQ4:2C4

4. ACCURACY STUDY OF MULTIPLIER REALIZED BY THE PROPOSED COMPRESSORS

In the accuracy metrics considered in this paper are introduced. Next, the accuracy of 8-, 16-, and 32-bit Dadda multipliers realized by the proposed compressors is studied. A proper combination of the proposed compressors may be utilized to achieve a better tradeoff between DQ4:2C4 for the LSB and MSB parts in the multiplication respectively, is suggested here. The results for this multiplier are denoted by DQ4:2Cmixed. These multipliers are compared by the approximate Dadda multipliers implemented by two prior proposed approximate 4:2 compressors discussed as well as the configurable multiplier suggested the accuracy and design parameters.

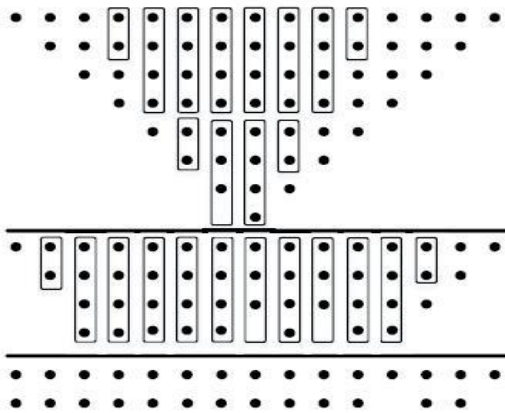


Figure 7: Dot diagram of proposed System

The general structure of the reduction circuitry in an 8-bit Dadda multiplier, which makes use of 4:2 compressors.

4.1 Error Evaluation Analysis Method:

In this section, an error evaluation analysis of the partial product perforation technique is presented. We evaluate the induced error metrics proposed, i.e., ED, MED, and NMED, as effective metrics for quantifying the accuracy of approximate arithmetic circuits.

- ED is defined as the absolute distance of the fully accurate product P and the approximate one P' , $ED = |P - P'|$
- The MED is the average of ED.
- The NMED for using MED is the average of EDs for all inputs and $NMED = MED/P_{max}$, where $P_{max} = (2n - 1)2$ in the case of an n -bit multiplier.

When applying the product perforation on an n -bit multiplier using SPP (Simple partial products) generation,

- ED of multiplying two numbers A and B is calculated as follows:

$$ED(A, B) = |P - P'| = A \sum_{i=0}^{n-1} b_i 2^i - A \sum_{i \notin [j, j+k)}^{n-1} b_i 2^i$$

$$= A \sum_{i=j}^{j+k-1} 2^i b_i = A 2^j x_B$$

- MED is calculated If p_A and p_B are the probability density functions (PDFs) of A and B , respectively,

$$MED = \sum_{\forall A, B} p_A(A) p_B(B) ED(A, B)$$

- NMED for using MED is the average of EDs for all inputs

$$NMED = \frac{MED}{(2^n - 1)^2} = \frac{2^j (2^k - 1)}{4(2^n - 1)}$$

4.2 Error Correction Methods:

In this section, we introduce two methods to decrease the error induced from the application of partial product perforation. They are implemented as extra components complementing the multiplication circuit, thus their area, power, and delay overheads as well as the error reduction they offer, do not depend on the architecture of the multiplier. Although multiplication is commutative, i.e., $A \times B = B \times A$, this does not apply in perforated multipliers. when multiplying $A \times B$, the imposed error is proportional to the multiplicand A and the term x_B and thus decreasing one of these operands decreases the error delivered to the output. As a result, comparing A and B or x_A and x_B before the multiplication and swapping accordingly, A and B can reduce the error.

5. RESULTS

Results of this paper is shown below

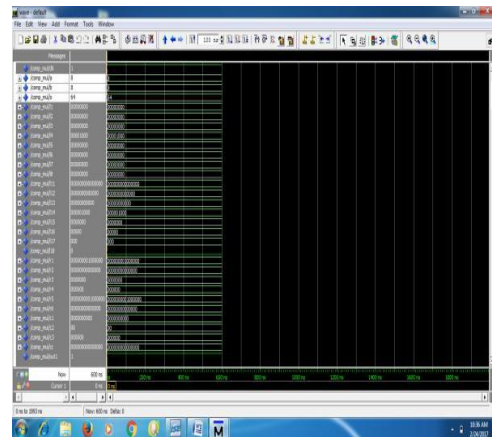


Figure 8: Accurate multiplier using 4:2 compressors

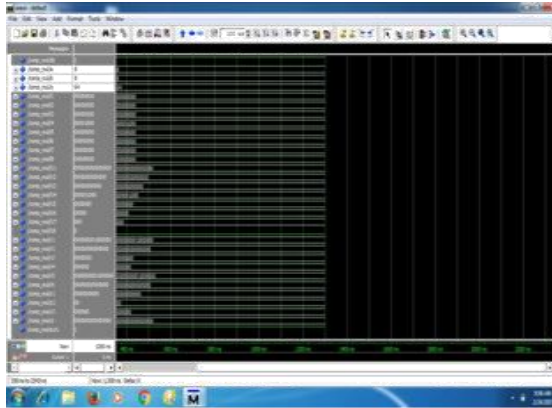


Figure 9: approximate multiplier using dual quality for 4:2 compressor

Table1: Tabulation

Multiplier	Power	Logic level
Multiplier using exact 4:2 compressors	25mW	3176 gates
Multiplier using approximate 4:2 compressors	7mW	1987 gates

6. CONCLUSION

In this paper we presented four DQ4:2Cs, which had the flexibility of switching between the exact and approximate operating modes. In the approximate mode, these compressors provided higher speeds and lower power consumption at the cost of lower accuracy. Each of these compressors had its own level of accuracy in the approximate mode as well as different delays and power in the approximate and exact modes. These compressors were employed in the structure of 32 bit Dadda multiplier to provide a configurable multiplier whose accuracy (as well as its power and speed) could be changed dynamically during the runtime.

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