A MAXIMUM LIKELIHOOD DECODING ALGORITHM FOR REDUCING THE COMPLEXITY OF LDPC CODE CORRECTION TECHNIQUE

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A**bstract--**In this paper, high linear architectures for verifying the first two maximum or minimum values are of utmost importance in several uses, including iterative decoders. The min-sum giving out step is to that it produces only two different output magnitude values irrespective of the number of incoming bit-to check communication. These new micro-architecture structures would utilize the minimum number of comparators by exploiting the concept of survivors in the search. These would effect in a reduced number of comparisons and consequently reduced energy use. Multipliers are complex units and play a major role in finding the whole area, speed and power consumption of digital designs. The parameters like latency, complexity and power consumption can be reduced by using the multipliers. The decoding algorithms we include generalize and unify the decoding schemes originally presented the product codes and those of low-density parity-check codes.

Index Terms: Check –node (CN) processing, Highrate, Highspeed, Layered schedule, Message Compression, NB-LDPC, trellis min-max (T-MM), VLSI design.

1. INTRODUCTION

Nonbinary low-density parity-check (NB-LDPC) codes are a actual kind of linear block codes defined over Galois fields (GFs) GF (q = 2p) with p >1. NB-LDPC codes have lot of advantages over its binary counterparts, which include much better error correction performance for short/medium code word length, higher burst error correction capability, and enhance the performance in the error-floor region. The key disadvantage of NB-LDPC codes is the high complexity of the decoding algorithms and the derived hardware architectures, which limit their application in actual scenarios where high throughput and reduced silicon area are important requirements.The main drawbacks of T-EMS, T-MM, and OMO-TMM are: 1) the high number of replaced messages between the CN and the VN (q × dc reliabilities), which influence in the wiring congestion, limiting the maximum throughput achievable and 2) the high amount of storage elements required in the hardware execution of these algorithms, which assumes the chief part of the decoder's area. This reduction in the messages introduces a performance loss in the coding gain that can be controlled by means of the parameter L. NB-LDPC codes are decoded applying iterative algorithms where messages that represent reliability values are passed from VN to CN and vice versa.

Extended min-sum (EMS) and min–max algorithms were planned with the aim of reducing the complexity offered by the solutions established on QPSA. Here in these algorithms, the CN equations are simplified by making approximations to involve only additions and comparisons in their parity-check equations. Since both the algorithms make use of forward–backward (FB) metrics in the CN processor and the maximum throughput is bounded due to the serial computations. Then the number of exchanged messages between CN and variable node (VN) for both the algorithms is nm × dc, where nm is a fraction of q total reliabilities, nm _ q, and dc the CN degree. Therefore, the number of messages between the nodes is lower than the previous solutions from the literature.

Improvements are based on QSPA, such as Fast Fourier Transform-SPA, log-SPA, and max-log-SPA; reduce the computational load of the parity- check equations without introducing any performance loss. The upcoming proposed trellis max-log-QPSA algorithm improves considerably both the area and the decoding throughput compared with the previous solutions based on the QPSA, making use of a path construction scheme to generate the output message in

the check-node (CN) processor. These solutions offers the highest coding gain for a high-rate NB-LDPC codes, but at the same time, they include costly processing that limits their application in real communication and storage systems.

2. EXISTING SYSTEM

2.1INTRODUCTION

The analysis of the algorithm then views on the work required for the merging process, because it is the merge work needed for a given subdivision scheme that originaly determines the growth of complexity. In this we introduce a recursive approach to the construction of codes which generalizes the product code construction and produce that the design of algorithms for encoding and decoding is processing to the first techniques of complexity theory. Long codes are develop from a bipartite graph and one or more sub codes; a new code is defined explicitly by its decomposition into smaller sub codes. These sub codes are then used by the decoder as centres of local half computations that, when accomplished iteratively, correct the errors. The decoding algorithms we propose generalize and unify the decoding schemes originally presented the product codes and those of low-density parity-check code. Furthermore, the correct choice of the transmission order for the bits can guarantee good performance against burst errors or a mixture of burst and random errors.

2.2 PROJECT DESCRIPTION

NON-BINARY low-density parity-check (NB-LDPC) codes are an original kind of linear block codes defined over Galois fields (GFs) GF (q = 2p) with p >1. NB-LDPC codes have lot of advantages over its binary counterparts that includes better error correction performance for short/medium code word length, highest burst error correction capability, and the enhanced performance in the error-floor region.

2.3 T-MM DECODING ALGORITHM WITH COMPRESSED MESSAGES

A thin parity-check matrix **H** defines that an NB-LDPC code, where each nonzero element h m ,n belongs to a GFs GF(q = 2p). Another common way to characterize the NB-LDPC codes is by means of a Tanner graph, where two kinds of nodes are separated representing all N columns (VNs)and M rows (CNs) of **H**. N(m) denotes the set of VNs connected to a CN m and M(n) denotes the set of CNs connected to a VN n; therefore, the cardinality of the sets corresponds to dc and dv .

2.4 T-MM ALGORITHM WITH REDUCED SET OF MESSAGES

In this section, we introduce a new method to reduce the number of messages exchanged between the CN and the VN compared with the offer from [11]. First, we define the reduced set of compressed messages that are sent from CN to VN and an approximation to obtain the rest of the values in the VN. Then the second, the performance of the method is examined. Third, a technique to generate the most reliable values of the set I (a) without building a complete trellis structure is presented

2.4.1 Reduction of the CN-to-VN Message

The sets I (a) and P(a) are required to generate the messages like Rm,n(a) at the VN processor, as shown in (3). Reducing the cardinality of the I (a), and the P(a) is also reduced. Hence our proposal is to keep the L most reliable values of I (a) and the corresponding ones of P(a) and E(a), where L < (q −1).Defining the complementary set a__ ∈a \ a_, we propose that the set E∗(a__) = m1(a__). Thus, the cardinality of the set E∗(a) is kept in q −1. Table I includes the number of bits of each one of the sets exchanged from the CN-to-VN processors that compared with the proposal from [11], where w is the number of bits used to quantize the reliabilities.

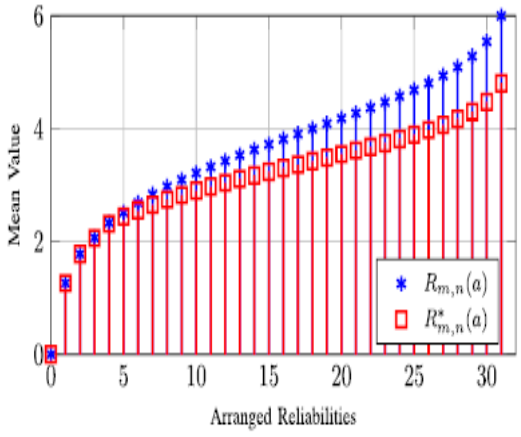


Figure 1: Mean value of each reliability

2.5CONCLUSION

The main drawbacks of T-EMS, T-MM, and OMO-TMM are: 1) the high number of replaced messages between the CN and the VN (q × dc reliabilities), which effects in the wiring congestion, reducing the maximum throughput possible and 2) the high amount of storage elements required in the hardware realization of these algorithms, and which expects the major part of the decoder's area. Thus to overcome the problems of the T-EMS and T-MM, the scheme in [11] introduces a technique of message density that reduces the wiring congestion between the CN and the VN and the storage elements that used in the derived architectures. These messages at the output of the CN are decreased to four sets that include the intrinsic and extrinsic information, the path directs, and the hard-decision symbols.

3. PROPOSED SYSTEM

The block diagram for the proposed CN is detailed in Figure 2 The CN input messages are **Q m**, **n**, which come from the VN processor and that unsure the hard-decision symbols **z**. Then both the input messages are used to compute the normal to- delta-domain transformation (**N** →_ block in Fig 4.1). Thus DC transformation networks are needed in the CN, each one requires q × log(q) w-bit MUX following the approach proposed in [19], where the w is the number of bits for the data path. **Z** is also used to gain the syndrome β adding all dc tentative hard-decision symbols. This operation requires w × (dc − 1) XOR gates.

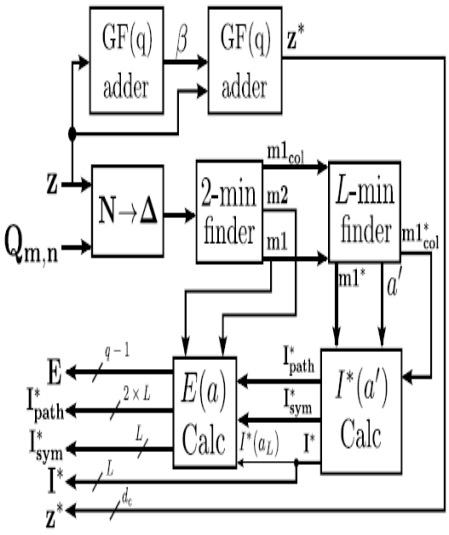
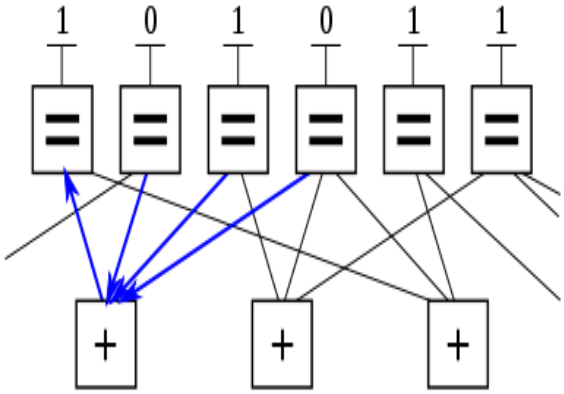


Figure: 2 proposed check node Block Diagram

B is used to generate the new hard has decision symbols **z**∗, which are sent to the VN to generate the R∗ m,n messages using (4). **Z** ∗ symbols are generated using GF(q) adders that require dc × w XOR gates to implement them.

3.1 DECODING

As with other codes, optimally decoding an LDPC code on the binary symmetric channel is the NP-complete problem, although techniques based on iterative belief propagation used in practice lead to obtain a better approximations. In contrast, that the belief propagation on the binary erasure channel is usually simple where it consists of iterative constraint fulfillment. For example, consider that the valid code word, 101011, from the example, is transmitted across a binary elimination channel and received with first and fourth bit erased to yield. Since the transmitted message must have full fill the code constraints and the message can be organized by written the message on the top of the factor graph. From this example, the first bit cannot yet be recovered, because all of the constraints connected to it have more than one of the unknown bit. Hence in order to proceed with decoding the message, this procedure may then iterate. Then the new value for the fourth bit can now be used in conjunction with the first constraint to recover the first bit as shown below. This shows that the first bit must be a 1 to satisfy the leftmost constraint.



Therefore, the message can be decoded iteratively. For the next channel models, the messages passed inside the variable nodes and check nodes are real numbers, which express probabilities and possibility of belief. This result can be validated by multiplying the corrected code word by the parity-check matrix **H**:

$$\mathbf{z} = \mathbf{Hr} = \begin{pmatrix} 1 & 1 & 1 & 1 & 0 & 0 \\ 0 & 0 & 1 & 1 & 0 & 1 \\ 1 & 0 & 0 & 1 & 1 & 0 \end{pmatrix} \begin{pmatrix} 1 \\ 0 \\ 1 \\ 0 \\ 1 \\ 1 \end{pmatrix} = \begin{pmatrix} 0 \\ 0 \\ 0 \end{pmatrix}.$$

Since the outcome **z** (the syndrome) of this operation is the 3 × 1 zero vectors, the resulting code word is successfully validated.

3.1.1Lookup table decoding

Then it is possible to decode LDPC codes on a relatively low-powered microprocessor by the use of lookup tables.

Whilst codes such as LDPC are generally executed on high-powered processors, with long block lengths, there are also applications which use lower-powered processors and short block lengths.

3.1.2Code construction

For large block sizes, LDPC codes are commonly constructed by first studied the behaviour of the decoders. Since, the block size which tends to infinity, then LDPC decoders can be shown to have a noise threshold below which decoding is really attained, and above which decoding is not achieved. This threshold can be optimised by finding the best proportion of arcs from check nodes and arcs from variable nodes. An approximate graphical approach to imagining this threshold is an EXIT chart.

4. CMOS TECHNOLOGY

4.1 Basic concepts

Ideally, a transistor performs like a switch. For NMOS transistors, if the input is 1 the switch is on, otherwise it off. Similarly, for the PMOS, if the input is 0 then the transistor is on, else the transistor is off.

4.2 N-Well CMOS Technology

- Process starts with a moderately tamper with (1015 cm-3) p-type substrate (wafer)
- An initial oxide layer is grown on the whole surface (barrier oxide)

4.3Metallization mask

- Aluminium is deposit over on the wafer and selectively etched
- The step exposure in this process is most critical (nonlinearity of the wafer surface)

4.4 ADVANTAGES

High input impedance. The input signal is driven electrodes with layer of insulation (the metal oxide) between them and what they are adjusting. This gives them a minor amount of capacitance, but almost infinite resistance.

- The outputs are dynamically driven both ways
- The outputs are much extra rail-to-rail
- CMOS logic takes very little power when held in a static state. The current consumption comes from the switching as both capacitors are charged and discharged. Even then, it has a better speed to power ratio equated to other logic types.
- CMOS gates are very simple the basic gate is an inverter, which is only two transistors. This always with low power consumption that means it lends itself well to dense integration.

4.5 Applications

- Transmission gates may be used in the analog multipliers
- CMOS Technology may also widely used in the RF circuits.

5. SIMULATION RESULT

The simulation environment is created in MODELSIM by using VERILOG language for the training. We consider the four systems which are in active, sleep, deep sleep and idle mode correspondingly. The power manager system calculates the required power to send the data to the subsystems. Normally we can send heavy or large amount of data to the system which is in the active mode.

- DC signal and Inverter is given as a input to the NAND gate .Clock frequency given as NAND gate for simulation output.
- Q BAR, QBAR1 be the output signal.

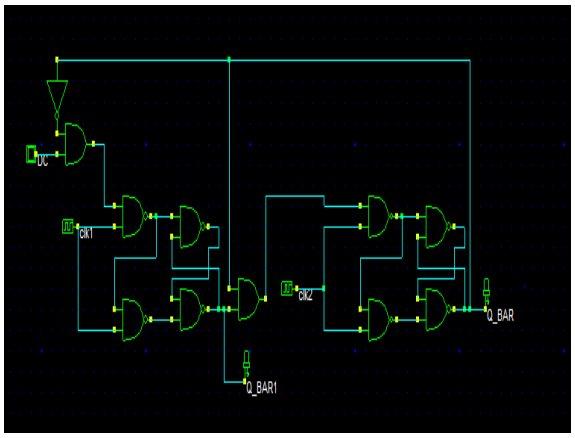


Figure 3: Digitalschematicforcircuittoextractthej[th] minimum value

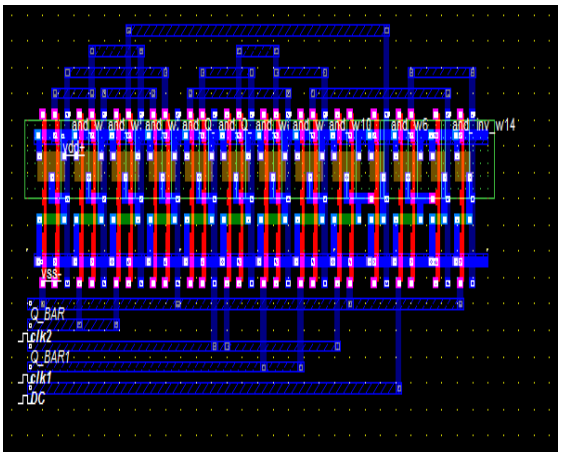


Figure 4: Design Layout for the output waveform

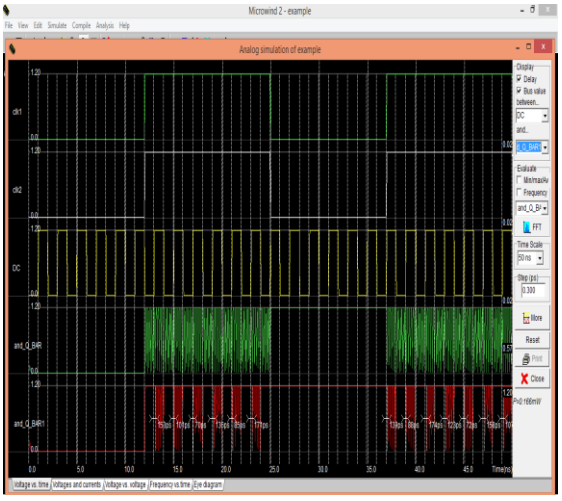


Figure 5: Simulation result for voltage vs time.

Figure 6: Simulation result for voltage and current

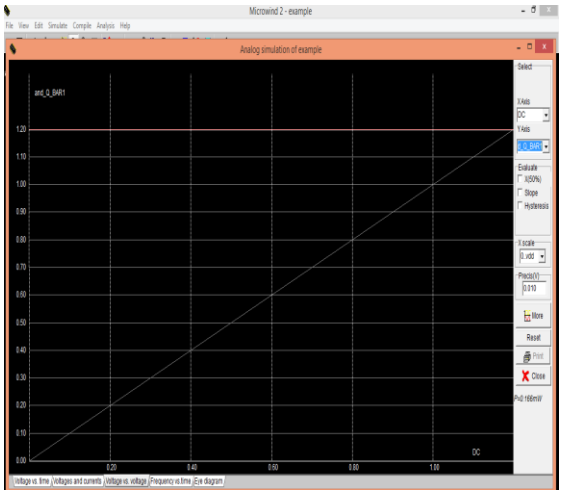


Figure 7: Simulation Result for voltage vs voltage

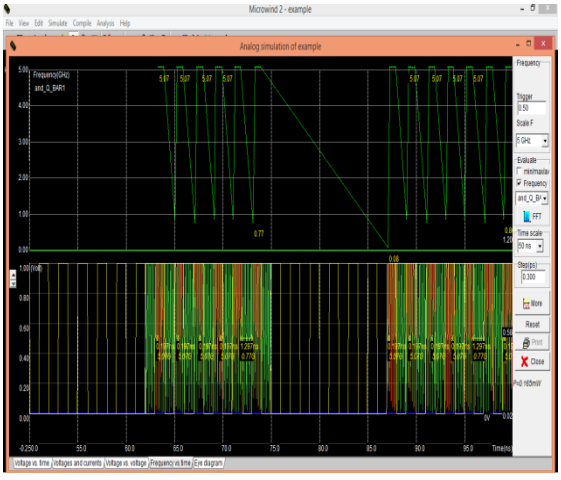


Figure 8: Simulation result for frequency vs time

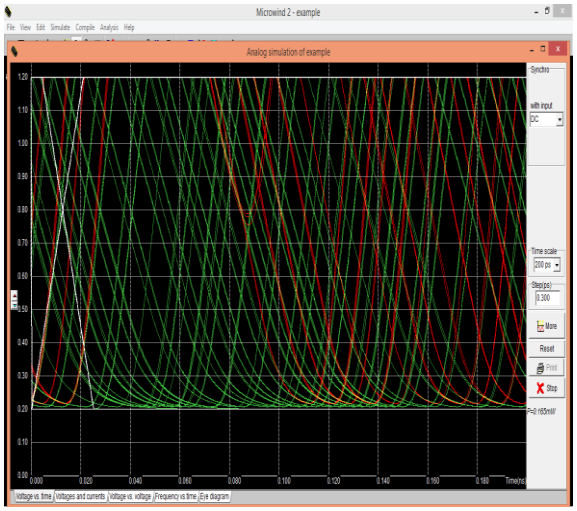


Figure 9: Simulation result for eye diagram

6. CONCLUSION AND FUTURE ENHANCEMENT

The low complexity design is prominent requirement of iterative decoders. We have tried to propose a design that fulfils the obligation with the completion of the sum min worker using better architecture. The difficulty is reduced as the number of register and memory utilization decreases.

NB-LDPC codes are designed using CMOS Technology. It concludes the T-MM algorithm to reduce the complexity of CN architecture. Hence the power consumption is decreased. In future, LDPC codes can be used for reduce the power consumption. Thus, the post creation throughput of the other works is reduced in the same percentage.

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